Energy-Efficient Indirectly Heated Phase Change RF Switch

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***Abstract*— Linear radio-frequency (RF) switches are highly desired in wireless system front ends. Here, we report electro-thermal measurements and modeling of an indirectly heated phase change RF switch (IPCS). We study the energy-efficiency of the IPCS device by electro-thermal modeling and show that its layer design is crucial to reduce its switching power. Thermally optimized SbTe-based IPCS devices switch at a record-low power of ~8 mW/μm^2, approaching the efficiency limit of such indirectly heated devices.**

***Index Terms*— Phase-change, RF switch, thermometry, power handling, energy-efficiency, SbTe.**

I. Introduction

THE demand for higher data rates and spectral efficiencies in wireless systems will make radio frequency (RF) front-ends more complex and challenging, e.g. with massive multiple-input-multiple-output antennas. In this context, linear RF switches with low insertion loss, high isolation and CMOS compatibility are desired [1]. Currently, silicon-on-insulator (SOI) RF switches are widely used [2]. RF SOI switches have achieved figure of merit (FOM) $= 1/(2\pi R_{on}C_{off}) \sim 1.5$ THz [2].

Phase change materials (PCMs) have been studied for non-volatile memory [3], [4], but are now being evaluated as RF switches [1], [5]–[13]. Phase change switches (PCS) have shown excellent FOM at 1 to 12 THz [5]–[12] for GeTe and SbTe, with switching endurance up to 10^7 cycles [12]. As the phase transition is induced thermally, power and heat management remain major challenges. For example, GeTe PCM amorphization requires heating the material above its melting temperature $T_M > 700$°C [4]. Thus, power and energy-efficiency of PCS are strongly dependent on their thermal design and the PCM alloy composition.

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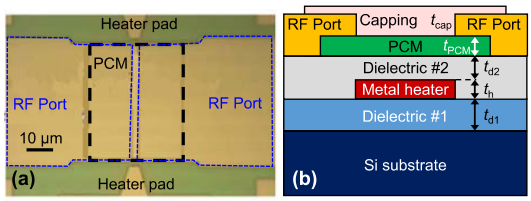

Fig. 1. **IPCS device.** (a) Optical image and (b) schematic cross-section of the 4-terminal IPCS device. The TiW heater is deposited on thermally grown SiO_2 (dielectric #1) on Si substrate. Dielectric #2 (SiN_x) electrically isolates the PCM (here Sb_7Te_3) from the metal heater. The PCM can be switched between high (amorphous) and low (crystalline) resistance states by Joule heating the metal heater.

In this letter we discuss energy-efficiency in the class of PCS where heating is induced *indirectly* by a refractory metal line heater. We first develop an electro-thermal model, calibrated by electrical thermometry and then explore design trade-offs. We find that the switching power can be reduced from ~25 to 5 mW/μm^2 by optimizing the layer structure and thicknesses. The improved energy-efficiency is experimentally demonstrated in SbTe-based indirectly-heated PCS (IPCS), where the thermal cycle temperature requirement is reduced to ~540°C. With the thermal layer optimization, state-of-the-art RF performance (~5 THz FOM) and excellent endurance of 10^7 were demonstrated [12]. We further discuss the energy-efficiency in a broader context and compare the IPCS with conventional *directly* heated vertical PCM (V-PCM) devices.

II. Electro-Thermal Measurements and Model

The IPCS device structure is presented in Fig. 1, same as the high isolation switch reported in [12]. A TiW line heater (with multiple simulated thicknesses t_h from 40 to 100 nm) is sputtered on dielectric #1 (here thermal SiO_2, simulated thickness t_{d1} from 50 to 250 nm) on a high-resistivity Si substrate. Dielectric #2 (SiN_x, thickness range t_{d2} from 40 to 100 nm) electrically isolates the PCM from the heater. The PCM is RF-sputtered Sb_7Te_3 [14] with thickness t_{PCM} from 40 to 100 nm. Ti-based Ohmic contacts are formed for the PCM, and the obtained RF performance was reported elsewhere [12].

First we measured the temperature coefficient of electrical resistance (TCR $= 4.3 \times 10^{-4}$ K^{-1}) of the TiW heaters using transfer length method (TLM) structures with widths $W =$ 2 to 6 μm and lengths $L = 4$ to 64 μm. Figure 2(a) shows the temperature-dependent TLM results: the electrical contact resistance (to TiW) is independent of temperature (T) but the specific electrical resistivity of the TiW increases linearly with T up to 500°C. Knowing the TCR, the heater ΔT and its thermal resistance are obtained from changes in electrical

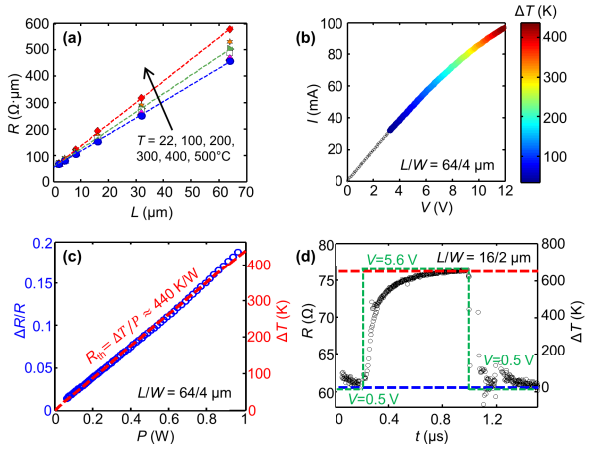

Fig. 2. **Electrical thermometry**. (a) Temperature-dependent TLM measurement of the TiW heater ($W = 5\ \mu$m) to determine its TCR. (b) Measurement of a heater with self-heating temperature extracted by converting ΔR to ΔT with the obtained TCR. (c) Measured relative ΔR (blue) and extracted $\Delta T = \Delta R/(R \cdot \text{TCR})$ (red) vs. heater power (P); power at the contacts ($2I^2R_C$) is subtracted. The slope represents the thermal resistance (R_{th}) of the heater line. (d) Transient measurement (black circles) of the resistance to probe the cooling time (ΔT obtained by TCR). A low DC bias of $V = 0.5$ V is applied to measure the resistance near room temperature and a voltage $V = 5.6$ V is pulsed between $t = 200$ ns and $t = 1\ \mu$s with rise and fall times of 20 ns (green dashed lines). Dashed red (blue) line represents the steady state R and ΔT during the 5.6 V (0.5 V) pulse.

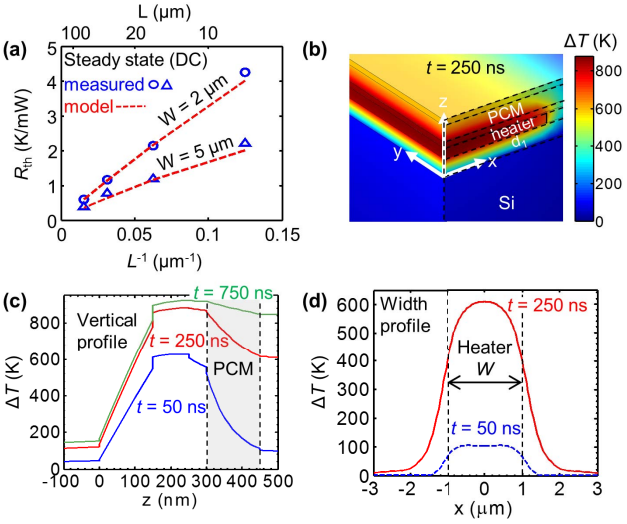

Fig. 3. **Electro-thermal model**. (a) Measured vs. simulated thermal resistance (R_{th}) of metal line heaters to calibrate the thermal model. The key fitting parameter is the TBR between TiW and SiO_2. (b) Representative temperature rise (ΔT) in IPCS at $t = 250$ ns with $P = 15$ mW/μm^2. (c) Vertical and (d) lateral ΔT profiles at 50 (blue) and 250 ns (red). The vertical profile also shows $t = 750$ ns (green, approaching steady state) and is taken at the center of the device ($x, y = 0, 0$). The width profile is at the top surface of the PCM layer ($y, z = 0, 450$ nm).

resistance ΔR, as shown in Figs. 2(b) and 2(c). We also used a Keithley 4200-SCS with 4225-PMU to measure the transient heater electrical resistance $R(t)$ shown in Fig. 2(d), but our measurement is limited by the electrical transient, setting only an upper bound on the thermal transient of the heater.

Figure 2(d) shows the heater is quenched from $\Delta T > 600$ K to <100 K in less than 250 ns. The thermal transient of the PCM can be evaluated using our simulations. In the IPCS device we can experimentally verify the amorphization process by measuring the (increased) resistance of the PCM.

Figure 3(a) summarizes the measured thermal resistance of our heaters (R_{th}, blue markers), comparing them to our electro-thermal model (red dashed lines) with good agreement. Four-terminal measurements were carried out to subtract the contact resistance, yet slight deviation between the model and measurements is seen for short heater length ($L < 8\ \mu$m) due to increased contribution of the contacts. Evidently, R_{th} scales linearly with the inverse heater length, L^{-1}. The key fitting parameter is the thermal boundary resistance at the TiW-SiO_2 interface, TBR ≈ 15 m^{2}K/GW in the measured temperature range (25-500°C), other thermal properties are given below.

The TiW thermal conductivity (10 Wm^{-1}K^{-1} near room T) and its T-dependence were estimated by the Wiedemann-Franz law from the measured electrical resistivity. Other thermal properties are taken from literature: $k_{Si} = 4 \times 10^4/T$ Wm^{-1}K^{-1}, $k_{SiO2} = \ln(T^{0.52}) - 1.6$ Wm^{-1}K^{-1} where T is in K [15]–[17]. For SiN_x $k_{SiN} = 3$ Wm^{-1}K^{-1} [18] and $TBR_{Si\text{-}SiO2} = 3$ m^{2}K/GW near room temperature for the Si-SiO_2 interface [19], making it negligible compared with the SiO_2. Thermal properties of the polycrystalline PCM are $k_{PCM} = 0.67$ Wm^{-1}K^{-1} [20] and $TBR_{PCM} = 25$ m^{2}K/GW near room temperature [21].

A representative simulated transient ($t = 250$ ns) ΔT distribution of the IPCS device is shown in Fig. 3(b). Vertical (z-axis) and width (x-axis) line profiles are shown in Figs. 3(c) and 3(d), respectively, at $t = 50$ ns (blue) and $t = 250$ ns (red). The vertical profile shows that for short pulses ($t <\sim 50$ ns) ΔT in the PCM is highly non-uniform because the heat does not have time to reach the top of the PCM. Hence, pulses shorter than τ_{th} will require more energy to switch the entire PCM layer, i.e. to reach $\Delta T > 600$ K at the top of the PCM. This thermal time constant (τ_{th}) is determined by the dielectric #2 and PCM layer thicknesses (t_{d2} and t_{PCM}) and thermal properties. It scales roughly as $\tau_{th} \sim (t_{d2} + t_{PCM})^2/\alpha$, where $\alpha = k_{th}/C_{th}$ is the thermal diffusivity (k_{th} is the thermal conductivity and C_{th} is the thermal capacitance). For example $\tau_{th} \sim 15$ ns in 100 nm thick SiO_x ($k_{SiOx} \sim 1$ Wm^{-1}K^{-1}, $C_{th,SiOx} \sim 1.45$ Jcm^{-3}K^{-1}).

The ΔT profile across the width is non-uniform as well due to the heat dissipation sideways (the 2 μm width of the buried heater is shown with dashed black lines). Thicker heater edges can balance the edge cooling (more current flow and more edge power dissipation), resulting in more uniform ΔT, but require an additional lithography step. We note that our model does not make any assumption on the TCR, which is measured in the range 25 - 500°C, and used to extract thermal properties as outlined earlier. The model assumes that the T-dependence of thermal properties does not vary significantly above 500°C, and the relevant temperature range is up to the melting temperature of the PCM (here ~540°C).

III. Energy-Efficiency and Trade-Offs

The finite element electro-thermal model by COMSOL Multiphysics allows us to explore various design trade-offs, and we focus here on the energy-efficiency of the reset process, namely programming the PCM to its amorphous (high resistance) state. We assume that PCM reset is achieved after its temperature exceeds the melting temperature ($\Delta T > 600$ K) during the pulse and it is quenched to $\Delta T < 100$ K in less than 250 ns after the pulse is turned off. We therefore wish to seek the balance between the minimum energy required to switch, while maintaining sufficiently fast cooling time.

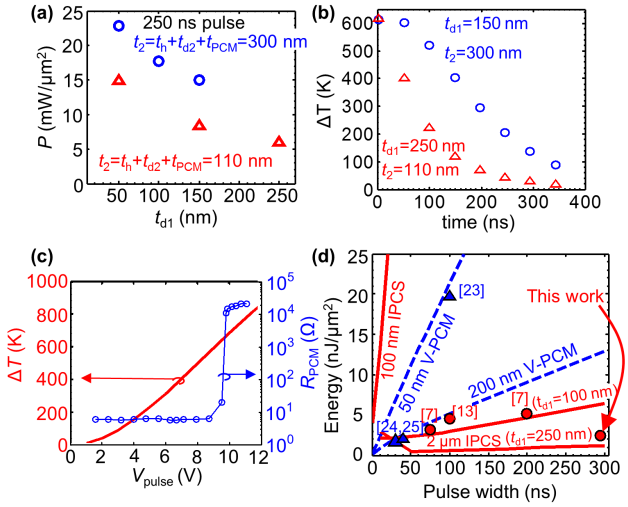

Fig. 4. **Design trade-offs and switching efficiency**. (a) Simulated power to reset (250 ns) vs. thickness of dielectric #1 (t_{d1}) for total thickness of heater (t_h), dielectric #2 (t_{d2}) and PCM (t_{PCM}) of t_2 = 300 nm (blue circles), same as in Fig. 3(c,d) and an optimized device with t_2 = 110 nm (red triangles). (b) Simulated cooling transient for two of the devices in (a) with t_{d1} = 150 nm and t_2 = 300 nm (blue circles) and t_{d1} = 250 nm and t_2 = 110 nm (red triangles). The most power efficient device from (a) can cool from $\Delta T \sim$ 600 K to $\Delta T <$ 50 K in $\sim$ 250 ns showing its ability to reset. (c) Measured PCM resistance (R_{PCM}, blue) and simulated ΔT at top of the PCM layer (red) vs. applied voltage pulse of 300 ns (V_{pulse}). (d) Energy to reset vs. pulse width. Lines are simulations of the IPCS (red solid) and V-PCM (blue, dashed). Blue symbols are experimental data points from [23]–[25]. Red circles are experimental measurements of IPCS from [7], [13], and this work (device with RF FOM $\sim$ 5 THz [12]). The indirectly heated IPCS cannot operate with pulse widths shorter than the diffusion time across the insulation and PCM layers (few ns, depending on device structure, dimensions, and materials).

Higher thermal resistance of the IPCS $R_{th} = \Delta T/P$ (where P is the applied power) is desired in order to reduce the reset power, yet the upper bound of this R_{th} is determined by the cooling rate required for the melt-quench process.

For convenient benchmarking we normalize the applied power by the heater area. Most heat is dissipated vertically (to the Si substrate heat sink) but some heat spreads laterally, hence devices which are small compared with the characteristic lateral thermal length (few hundred nm in our devices) are less efficient due to the lateral heat loss.

The thickness of the different layers is a key design variable. The thickness of dielectric #1 (t_{d1}), which separates the heater from the substrate, strongly affects the thermal resistance and should be maximized (for highest R_{th}) while still achieving sufficient cooling rate. Fig. 4(a) shows the simulated decrease in switching power with increased t_{d1}. The heater thickness (t_h) should be balanced between thinning to increase power density (increasing the effective R_{th}) and making it thicker to reduce the applied voltage (e.g. for CMOS compatibility). Dielectric #2 (t_{d2}) is needed for electrical isolation of the heater from the RF path and to reduce the off-capacitance (C_{off}), but thermally this must be thin, as it separates the PCM from the heater. Our simulations indicate that using a high thermal conductivity insulator for d_2 (e.g. AlN) [13] leads to more switching power because this layer acts as a heat sink, cooling the heater. This can be intuitively understood by noting that AlN is more thermally conductive than TiW ($k_{th,AlN} \sim 100$ Wm^{-1}K^{-1} [22] and $k_{th,TiW} \sim 10$ Wm^{-1}K^{-1}).

The PCM thickness should also be minimized in order to reduce the switching power and time, because the heat has to propagate to its top. On the other hand, reducing the PCM thickness increases the electrical resistance of the device, R_{ON}, so there is a trade-off between energy-efficiency and RF performance. The indirectly heated structure discussed here and in other RF switches [13] (which is necessary to separate the heating medium from the RF path) also includes a strong dependence on the thicknesses of the top layers (heater t_h, dielectric #2 t_{d2}, and PCM t_{PCM}).

The general thermal design guideline is that the thickness of layers above the heater should be minimized because the thermal time constant scales with the thickness squared ($\tau_{th} \sim t^2/\alpha$) due to the diffusive nature of heat propagation. This trend is reflected in Fig. 4(a) by the lower switching power for t_2 = 110 nm (red triangles) vs. t_2 = 300 nm (blue circles) for pulse width of 250 ns. The reduction in t_2 also improves the cooling time [see simulation in Fig. 4(b)] and the optimized layer thickness shows more than $\sim 3\times$ reduction in switching power compared with the baseline [Fig. 4(a)]. Figure 4(c) shows the measured R_{PCM} (blue) vs. applied voltage confirming the reset process. The simulated ΔT at top of the PCM layer (red) exceeds the melting temperature during reset, consistent with our thermal modeling based on the measured R_{th}.

We note that ΔT in Fig. 4(c) differs from that in Fig. 2(c), the former being for the PCM with pulsed voltage, the latter for the metal heater during DC operation. The switching power will scale roughly linearly with T_M, and our analysis is valid for the chalcogenide-based PCMs (Ge-Sb-Te system) for which $T_M \sim$ 540-720°C and $k \sim$ 0.5-1 Wm^{-1}K^{-1}. The exact value of T_M is not expected to significantly change our results; if, for example, ΔT required for melting is 600 K instead of 550 K it will change the power needed to melt only by <10%, whereas the improvement shown here by thermal design is more than a factor of 3×.

Figure 4(d) compares the switching energy (per area) of the IPCS (red) with conventional vertical phase change memory V-PCM (blue) at different lateral dimensions. Our simulations match the experimental data (symbols). *Indirect* heating devices, where the heat must propagate from the heater to the PCM, are inherently less efficient than *direct* heating devices such as V-PCM. This is especially evident at short pulses for which heat does not have sufficient time to reach the PCM layer in IPCS (for instance see the increase in energy for pulses shorter than ~50 ns with t_{d1} = 250 nm). References [26] and [27] show similar trade-off, with less power needed for longer pulse widths, although no reduction in power consumption is expected for pulses longer than the thermal transient (at thermal steady state). In addition, Fig. 4(d) shows that as lateral dimensions decrease, more energy per area is required to switch due to greater lateral heat loss.

IV. Conclusion

We presented an indirectly-heated phase change RF switch based on Sb_7Te_3, and discussed its energy-efficiency. An electro-thermal model calibrated with experimental data shows that proper layer design is crucial to reduce the switching power. Particularly, the dielectric under the heater must be optimized to thermally isolate the heater from the substrate while allowing for sufficiently fast cooling, and layers above the heater should be thermally thin. Such optimized IPCS devices switch at record-low power and energy density of ~8 mW/μm^2 and ~2.4 nJ/μm^2, respectively, with RF FOM of ~5 THz.

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