Nano Research 2016, 9(10): 2950–2959
DOI 10.1007/s12274-016-1180-0
Research Article
ISSN 1998-0124
CN 11-5974/O4

SANTA: Self-aligned nanotrench ablation via Joule heating for probing sub-20 nm devices

Feng Xiong[1,†] (✉), Sanchit Deshmukh[1], Sungduk Hong[2], Yuan Dai[2], Ashkan Behnam[2], Feifei Lian[1], and Eric Pop[1] (✉)

[1] *Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA*
[2] *Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA*
[†] *Present address: Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, PA 15261, USA*

Received: 14 May 2016
Revised: 10 June 2016
Accepted: 13 June 2016

KEYWORDS
nanolithography,
carbon nanotubes,
graphene,
finite element,
self-aligned fabrication,
nanoscale thermal transport

ABSTRACT

Manipulating materials at the nanometer scale is challenging, particularly if alignment with nanoscale electrodes is desired. Here, we describe a lithography-free, self-aligned nanotrench ablation (SANTA) technique to create nanoscale "trenches" in a polymer like poly(methyl methacrylate) (PMMA). The nanotrenches are self-aligned with carbon nanotube (CNT) or graphene ribbon electrodes through a simple Joule heating process. Using simulations and experiments we investigated how the Joule power, ambient temperature, PMMA thickness, and substrate properties affect the spatial resolution of this technique. We achieved sub-20 nm nanotrenches, for the first time, by lowering the ambient temperature and reducing the PMMA thickness. We also demonstrated a functioning nanoscale resistive memory (RRAM) bit self-aligned with a CNT control device, achieved through the SANTA approach. This technique provides an elegant and inexpensive method to probe nanoscale devices using self-aligned electrodes, without the use of conventional alignment or lithography steps.

1 Introduction

One-dimensional (1D) materials such as nanowires (NWs) [1, 2], carbon nanotubes (CNTs) [3, 4], and graphene nanoribbons (GNRs) [5–7] have attracted much interest due to their interesting mechanical, electrical, and thermal properties in comparison to bulk materials. CNTs and GNRs specifically have been actively considered for electronic applications because of their nanoscale dimensions and high current-carrying capabilities [8]. CNTs and GNRs could also be used as extremely sharp nanoscale electrodes for other nanoscale materials such as molecules [9], DNA [10], and memory bits [11]. In order to probe such nanomaterials, it is crucial to align the CNT or GNR with the object being probed, and to achieve this with nanoscale resolution. Although electron-beam (e-beam) lithography could, in principle,

Address correspondence to Feng Xiong, fxiong@stanford.edu; Eric Pop, epop@stanford.edu

be used to create patterns with nanometer-scale spatial resolution, it is time-consuming and expensive, and alignment to individual CNTs (1–2 nm diameter) would be extremely challenging.

In a previous study, we proposed a simple mechanism for utilizing Joule heating from CNTs in order to pattern nanoscale "trenches" in a polymer [12]. Similar lithography-free techniques have also been proposed for sensor applications [13], for the study of biological and chemical phenomena [14], catalytic NW growth [15], and selective removal of metallic CNTs [16]. Localized heating has also been used as a simple patterning approach for nanoscale positioning [17–19]. Microheaters have been studied for selective functionalization of sensors [20] and catalytic synthesis of nanomaterials [18]. The advantage of using CNTs as Joule patterning electrodes is that given their small diameter (1–2 nm), nanoscale patterns ought to be achievable. However, only patterns of ~50 nm width were realized in previous work, and a deeper understanding of how to create and optimize such nanoscale features by Joule heating has been lacking until now.

In this work, we push the Joule patterning method towards ~10 nm scale features, achieved through a deeper understanding and optimization of nanoscale heating. We first present a three-dimensional (3D) finite-element method (FEM) model of Joule heating around a CNT covered by a polymer film. This provides a predictive platform revealing all variables controlling the formation of nanoscale features during heating. Guided by these simulations, we fabricated sub-20 nm nanotrenches in poly(methyl methacrylate) (PMMA) by tuning the input power, substrate temperature, and PMMA thickness. We also report successful nanopatterning with narrow two-dimensional (2D) graphene heaters, achieving ~30 nm width for the first time. Unlike conventional lithography techniques, the self-aligned nanotrench ablation (SANTA) technique automatically aligns the devices to be tested with the 1D or 2D probing electrodes. As a novel test case, we report a working nanoscale resistive random access memory (RRAM) bit self-aligned with a CNT control device, entirely fabricated through the SANTA approach.

2 Results and discussion

2.1 Process of forming nanotrenches

Figure 1 demonstrates the SANTA process and shows atomic force microscopy (AFM) images of the CNT heater and the nanotrench. We start with a CNT device with Pd electrodes on a SiO_2/Si substrate. The CNT growth and device fabrication steps were reported in detail elsewhere [21]. CNTs with different chiralities (metallic or semiconducting) and different diameters (single-walled or small diameter multi-walled) could all be used in the SANTA technique, as long as they pass a sufficiently high current to heat and pattern the PMMA (e.g. semiconducting CNTs need to be gated in the "on" state, while metallic CNTs can be used without gating). We spin coat a thin layer of PMMA on top of the CNT, with thickness varying from 20 to 60 nm, as controlled by the spin rate (see the Electronic Supplementary Material (ESM)). We

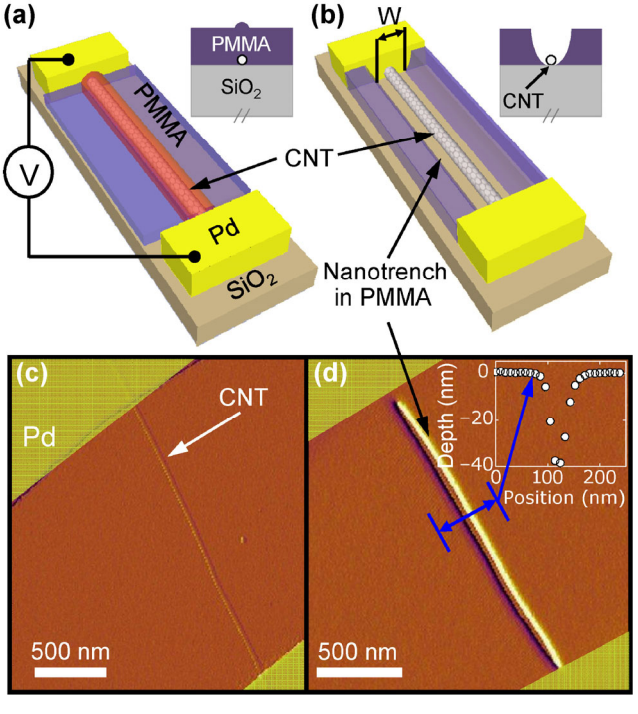

Figure 1 The SANTA technique: (a) Joule heating in the CNT leads to nanotrench formation in the PMMA covering the CNT, as the polymer evaporates. (b) The nanotrench is self-aligned with the CNT heater. Insets show cross-sectional views. (c) False-color AFM image of a CNT before PMMA deposition. (d) AFM image of the nanotrench formed in PMMA. Inset shows depth profile across the nanotrench, measured by AFM.

then apply a constant voltage across the electrodes to induce current flow in the CNT. Joule heating from the CNT heats the PMMA film (Fig. 1(a)) causing it to ablate, leaving behind a nanotrench self-aligned with the CNT (Figs. 1(b) and 1(d)). The insets in Figs. 1(a) and 1(b) show the cross-sectional view perpendicular to the CNT. The Fig. 1(d) inset shows the depth profile of the resulting nanotrench, with the CNT at its bottom.

We note that if the input power is insufficiently high, the nanotrench may not form along the CNT all the way to the two electrodes, due to heat sinking at the metal contacts [22, 23]. We perform the entire process in an environmentally controlled probe station (typically under ~10^{-5} Torr vacuum) to prevent CNT breakdown and control the substrate temperature. The resulting nanotrench provides a convenient platform to position active materials such as molecules for sensor and biological studies [9, 10, 14, 24], dielectric nanowires or memory bits [11, 12], and nanowires synthesized via catalytic growth or direct deposition [15, 18, 19]. The process can also be used to remove unwanted CNTs after plasma etching [16].

2.2 Simulation platform

To better understand the heating and temperature distribution in our devices, we developed a 3D COMSOL FEM model that is consistent with our experimental setup, as shown in Fig. 2(a). To improve the efficiency, only a quarter of the actual device is simulated, taking advantage of the two symmetry planes. Figure 2(a) shows that the first symmetry plane bisects the CNT into two half-cylinders along its axis; the second symmetry plane bisects the CNT in the middle, perpendicular to its axis. The second assumption is valid for metallic CNTs (which have uniform heating) and is a reasonable approximation for semiconducting CNTs under high bias [21]. The size of the simulated Si substrate is 20 μm × 20 μm × 20 μm, sufficiently large to capture all heat flowing away from the CNT, but small enough to facilitate meshing and computation [25]. The bottom surface and the two side surfaces (non-symmetry planes) are held at ambient temperature (isothermal boundary conditions), while all other outer surfaces are treated as thermally insulating (adiabatic boundary conditions).

Figure 2(b) shows a zoomed-in image of the CNT

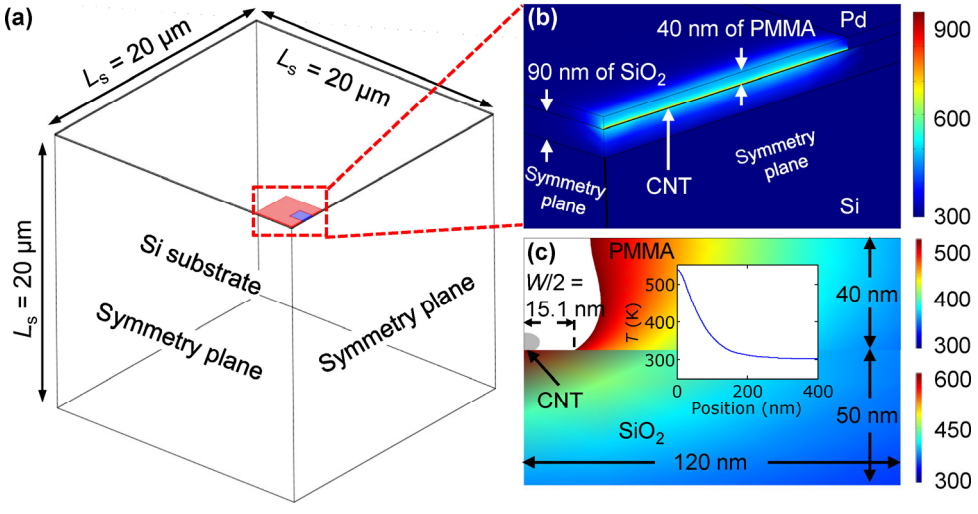

Figure 2 (a) Schematics of 3D heating model of the test structure. Only a quarter of the actual device is simulated, taking advantage of symmetry conditions. The highlighted region indicates the CNT heater. (b) Temperature profile in the device due to Joule heating from the CNT heater for ambient temperature T_0 = 300 K. (c) Cross-sectional temperature profile at the middle of the CNT. The white region represents the PMMA volume whose temperature exceeds the evaporation temperature of PMMA (~573 K). The nanotrench width W is defined as the narrowest region where all PMMA is heated above its boiling temperature. The CNT is drawn disproportionally large for clarity and two different temperature scales are used to better illustrate the temperature distribution in the upper (PMMA) and lower (SiO_2) regions, respectively. The inset shows the temperature profile away from the CNT heater, with a maximum temperature gradient of ~2.7 K/nm, similar to the temperature gradient of the nanowire heater reported by Jin et al. [18].

heater, and confirms that the greatest temperature gradients are very close to the CNT itself. The 3D model includes thermal boundary resistances (TBR) at all interfaces, matched against data from the literature. The lumped TBR at the CNT–Pd interface is $R_{th,c} \approx 1.2 \times 10^7$ K/W and a thermal boundary conductance $g = 0.17$ W/(K·m) (per CNT length) is applied at the CNT-SiO_2 boundary [26]. All other interior interfaces (Si–SiO_2, SiO_2–PMMA, and CNT–PMMA) have $R_{th} = 2.5 \times 10^{-8}$ m^2·K/W (per unit area) [7, 25, 27]. The thermal conductivities of the CNT, SiO_2, Si, PMMA, and Pd are taken as 2,200, 1.4, 150, 0.1, and 70 W/(K·m), respectively [7, 22]. The thermal model solves the steady-state 3D heat diffusion equation to obtain the temperature profile in the device. (The heat diffusion equation is appropriate without any ballistic corrections because the CNT is long and the materials immediately surrounding it are amorphous, with low thermal conductivity.) Figure 2(c) shows a typical cross-sectional temperature profile in the middle of the CNT (same orientation as the inset of Fig. 1(b)). The nanotrench is formed where the PMMA temperature exceeds its boiling point (~523 K), as shown by the void (white) region in Fig. 2(c). The inset shows the temperature profile along the lateral direction with a peak temperature gradient of ~2.7 K/nm. This confirms that the CNT heater creates a highly localized temperature profile and thus forms a nanoscale trench.

2.3 CNT heaters

As our next step, portrayed in Figs. 3 and 4, we systematically studied the effects of input power per unit CNT length (P_L), ambient temperature (T_0), PMMA thickness (t_{PMMA}), and substrate type on the width of the nanotrench (W). This width is defined as the narrowest region where all the PMMA is heated above its boiling temperature. Figure 3(a) shows how W varies as a function of the input power per unit length (P_L) at different ambient temperatures. Here, the PMMA thickness $t_{PMMA} = 40$ nm, and the CNT is on a 90 nm thick SiO_2 layer on a 500 μm Si wafer, consistent with our initial experiments. The dashed lines are FEM simulation results and symbols show the measured experimental results. The nanotrench widths were measured by AFM using sharp single crystalline diamond (SCD) probes with a tip radius ~5 nm, accounting for the tip convolution effect [28]. We varied the ambient temperature in steps of 50 K from 150 to 350 K for various CNTs that were otherwise subjected to similar conditions; different temperatures are color coded in the diagram.

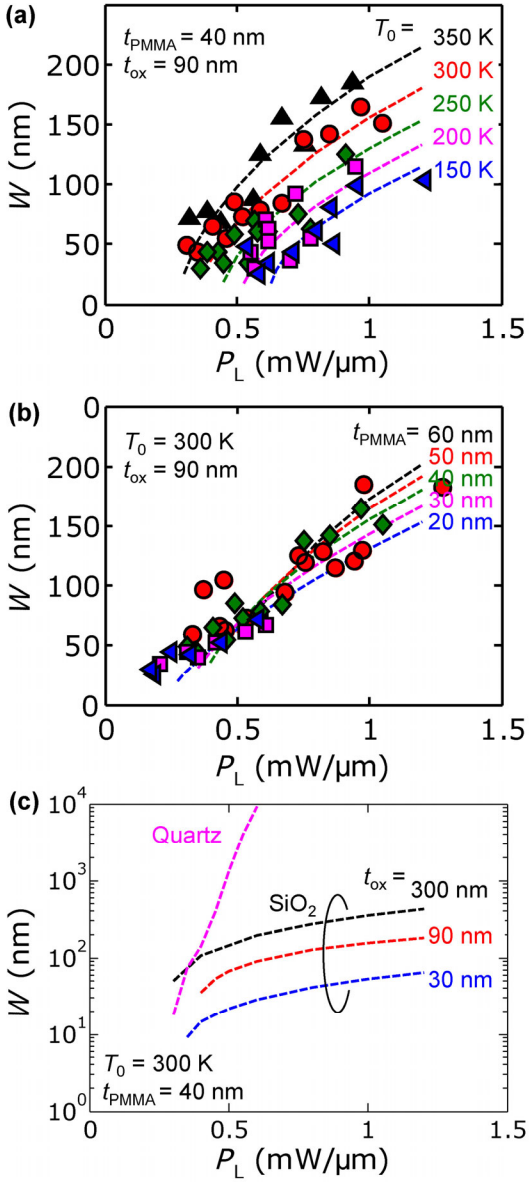

Figure 3 Nanotrench width in PMMA as a function of input power to the CNT heater. Dashed lines are simulation results from the COMSOL model. Symbols are experimental data. (a) Effect of ambient temperature on nanotrench width. (Thickness of PMMA is 40 nm; substrate is 90 nm SiO_2.) (b) Effect of PMMA thickness on nanotrench width. (Ambient temperature is 300 K; substrate is 90 nm SiO_2.) (c) Effect of substrate on nanotrench width. (Ambient temperature is 300 K; PMMA thickness is 40 nm.)

Our simulations generally agree with the experimental data, and most importantly the qualitative trends are confirmed: The nanotrench W increases sublinearly (almost logarithmically) with $P_L = I(V - I \cdot R_C)/L$, which excludes the voltage drops at the contacts. Here we estimated the electrical contact resistance R_C from the CNT resistance at low voltage, when R_C is expected to dominate for our process conditions [21]. The normalized Joule heating power (per length) P_L is a better parameter to quantify the ablation process than either applied voltage V or current I alone, since each CNT device may have different resistance, chirality, and channel length. While we could use either the constant voltage or constant current approach to achieve the desired input power density, we chose the constant voltage method in this work to limit the voltage across the CNT and avoid device breakdown. The sublinear dependence of W on P_L is not unexpected, because as the nanotrench grows in width, more heat (from the CNT) is lost to the underlying substrate than in heating the PMMA.

We also see that the power required to form a nanotrench of a given width decreases with increasing ambient temperature, as it is easier to heat up and evaporate PMMA at elevated temperatures. Thus, heating the substrate may be desired in applications when semiconducting CNTs cannot generate enough power to "burn" through a relatively thick layer of PMMA. At lower temperatures, nanotrench widths are naturally smaller for a given P_L, allowing us to achieve sub-20 nm wide nanotrenches at 150 K ambient. Qualitatively, at a lower temperature, only PMMA that is in close proximity to the CNT will be heated to sufficient temperature, thus producing a narrower nanotrench. At the same time, the viscosity of a liquid is generally lower at lower temperature, limiting the reflow of the PMMA film and assisting in keeping the width small.

We next examined the effect of PMMA thickness on CNT nanotrench width, as shown in Fig. 3(b). An ellipsometer was used to measure the PMMA thickness. In this case, the ambient temperature was 300 K and the substrate was 90 nm SiO_2. We controlled the PMMA thickness by varying the spin rate and/or adding A-thinner into the PMMA. Tabulated results of PMMA thickness as a function of spin rate and A-thinner concentration are included in the ESM. With thinner PMMA, the minimal achievable nanotrench width is smaller, as the minimal power to evaporate a thinner layer of PMMA is lower. From the simulation in Fig. 3(b), we also observed that the rate of increase of W with respect to the input power P_L is smaller for thinner films. This is beneficial, as it allows us to have better control over the nanotrench width and better tolerance of variation in input power. However, for applications where a lift-off process is necessary (e.g., depositing dielectrics, memory bits, or metal nanowires [12]), we cannot reduce the PMMA thickness below a certain value [29], depending on the type and thickness of the material deposited in the nanotrench.

We also looked at how different substrates may affect the temperature distribution and thus the nanotrench width around CNT heaters. In Fig. 3(c), we varied the SiO_2 thickness (t_{ox} = 30, 90, and 300 nm), and also looked at the temperature profile for the CNT sitting on a quartz substrate. The ambient temperature was 300 K and the PMMA thickness 40 nm. In the typical SiO_2/Si configuration, we see that with thinner SiO_2 the nanotrench width is significantly lower for the same input power. With thinner oxide, "vertical" heat dissipation from the CNT via the oxide to the thermally conductive Si substrate is increased. As a result, there is less lateral heat spreading from the CNT heater to the PMMA, resulting in a sub-10 nm nanotrench for 30 nm SiO_2 thickness (note the logarithmic vertical scale in Fig. 3(c)). However, if the CNT is placed on a quartz substrate (thermal conductivity ~10 W/(m·K)), the lateral heat dissipation is significantly larger. The trench width thus increases almost exponentially with P_L, because the entire quartz substrate is heated and therefore heats the PMMA from below (Fig. S3 in the ESM). Conversely, we note the unusual case of a thermally anisotropic substrate such as $La_5Ca_9Cu_{24}O_{41}$ (LCCO), which is thermally conductive in the vertical direction (~100 W/(m·K)) but insulating in the lateral direction (~2 W/(m·K)) [30], which could be an ideal choice for creating ultra-narrow trenches.

It is interesting to note that the nanotrench may take up to a few seconds to reach its steady-state width, as shown in Fig. S4 of the ESM. These times are much

longer than the thermal time constants of such a system (hundreds of nanoseconds) [27, 31], suggesting PMMA may reflow during this process. While our simulations cannot account for the complicated evaporation, melting, and reflow processes of PMMA, they nevertheless provide good agreement with the experimental data (Fig. 3). More importantly, these steady-state simulation results illustrate clearly how different parameters (input power density, ambient temperature, PMMA thickness, and substrate thermal resistance) affect the SANTA process and allow us to fine-tune these parameters to achieve a desired nanotrench width for different applications.

As stated earlier, these PMMA nanotrenches can be filled with other materials such as evaporated metals. After PMMA lift-off, this will then lead to the formation of a metal nanowire that is self-aligned with the CNT underneath. In Fig. 4(a), we show such a typical metal nanowire, generated from the nanotrench after metallization (Cr, 5 nm) and lift-off. Here the trench was formed by applying an input power $P_L \approx 0.47$ mW/μm along the CNT at 300 K. The CNT heater was on a 30-nm SiO_2 (on Si) substrate and was covered with 40 nm of PMMA. A scanning electron microscopy (SEM) image confirmed uniform coverage of the metal nanowire along the CNT. The inset reveals a zoomed-in high-resolution SEM image showing that the width of this nanowire was ~20 nm, consistent with our simulation predictions.

2.4 CNT-based memory devices

Because of the contact cooling effect, the temperature of the CNT which forms the nanotrench is lower near the metal contacts over a distance comparable to the so-called thermal healing length L_H along the CNT; here $L_H \approx 200$ nm [22, 23, 32]. Thus, depending on input power, a nanotrench may not always form all the way to the metal contact, enabling the existence of a short CNT segment in series with the nanowire formed in the nanotrench.

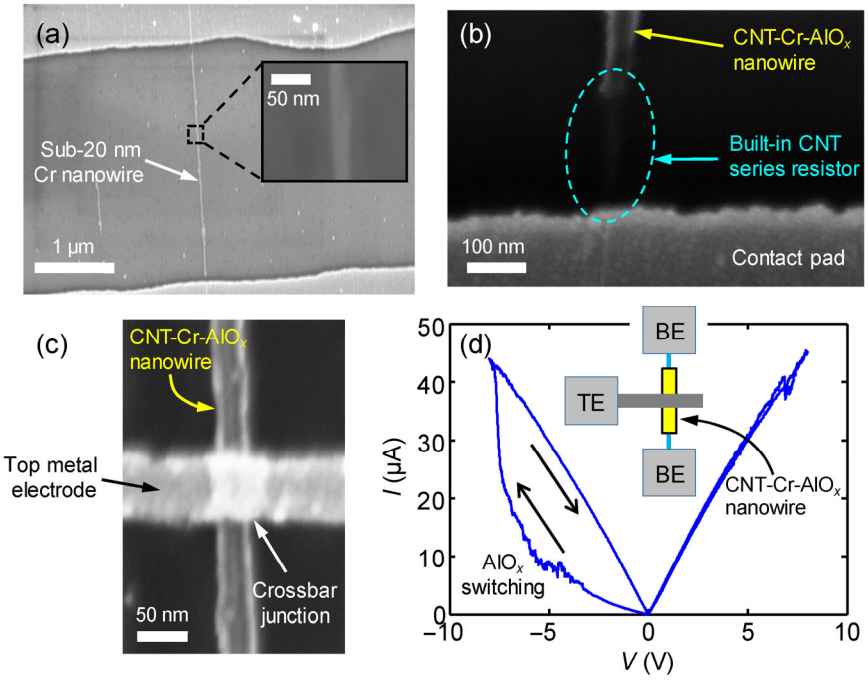

Figure 4 Building coaxial nanowires and RRAM devices with the SANTA technique. (a) SEM image of a Cr nanowire formed along the CNT after metal evaporation and PMMA lift-off, showing uniform metal coverage of the CNT. Inset is a zoomed-in high resolution SEM revealing ~20 nm nanowire width. (b) SEM image of CNT-Cr-AlO$_x$ nanowire which does not span all the way to the metal contact. (c) SEM image of a crossbar memory (RRAM) device with the AlO$_x$ as the resistive switching material. The short uncovered CNT segment in (b) serves as a built-in series resistor and a selection device. (d) Measured current–voltage of the crossbar memory device. The inset is the schematic of the crossbar RRAM, where the CNT serves as the bottom electrode (BE). The top electrode (TE) is separately patterned.

Here we exploited this capability to demonstrate a novel device: a nanoscale RRAM device with a CNT built-in series resistor and selection device. By controlling the SANTA input power, we limited the nanotrench in the PMMA from reaching the contact. We then evaporated 5 nm of Cr followed *in situ* by 5 nm of AlO_x, without breaking vacuum. Performing PMMA lift-off, this yielded a CNT-Cr-AlO_x coaxial nanowire in series with a short CNT segment (protected by the intact PMMA near the contact), as shown in Fig. 4(b). The short CNT segment could serve the role of a current compliance resistor (if metallic) or selection device (if semiconducting) in RRAM applications, without additional fabrication steps. To enable electrical measurements, we finally patterned a top metal electrode (Ti/Pd, 2/30 nm) to form a crossbar RRAM device, as illustrated in the SEM image (Fig. 4(c)) and the schematics (Fig. 4(d) inset). As the applied electric field increases across the oxide, a filamentary conduction path forms in the otherwise-insulating AlO_x, resulting in a significant drop of the device resistance. In typical RRAM devices, this sudden drop in resistance may lead to a large increase in current density and possible thermal runaway. In this context, the built-in CNT segment acts as a current compliance resistor, as shown in the measured *I*–*V* characteristics (Fig. 4(d)).

2.5 GNR heaters

In addition to the 1D CNTs, we also used GNRs with widths varying from 30 to 400 nm, as heaters to demonstrate the broad usefulness of the SANTA technique. Detailed fabrications of GNRs are reported elsewhere [33]. In short, we grow single-layer graphene samples on Cu foils by chemical vapor deposition (CVD), transfer them onto 90 nm SiO_2 substrates (on Si), and pattern them into ribbons by e-beam lithography. The electrode pads are Ti/Au (0.5/30 nm). A schematic of a typical GNR device is shown in the Fig. 5(b) inset. Figure 5 shows experimental (symbols) and simulation (dashed lines) results of GNR nanotrench formation, with different GNR widths (30, 60, 200, and 400 nm). The PMMA thickness and SiO_2 thickness are 40 and 90 nm, respectively.

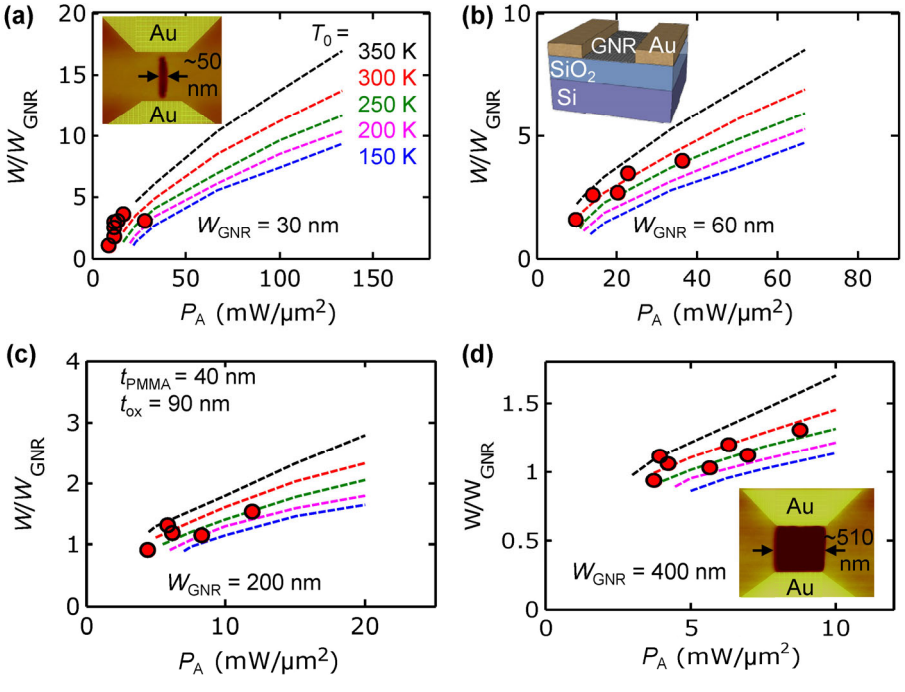

Figure 5 Patterning of nanotrenches into PMMA using GNR heaters. Plots show nanotrench width normalized by GNR width as a function of input power per unit area (P_A) in GNRs at different ambient temperatures (150 to 350 K from bottom to top). The PMMA thickness is 40 nm and the substrate is 90 nm SiO_2. Dashed lines show COMSOL simulation results and symbols show experimental data at 300 K. (a)–(d) GNRs with width of 30, 60, 200, and 400 nm, respectively. Insets in (a) and (d) are false-color AFM images of nanotrenches in PMMA after Joule heating in the GNRs. The inset in (b) shows the schematic of a GNR device.

As the heater dimension goes from 1D (CNTs) to quasi-2D (GNRs), the general trends still hold, i.e. the nanotrench width grows sub-linearly with the input power and the nanotrench width is smaller for lower ambient temperatures. As the GNR heater width increases, the minimum achievable nanotrench width increases accordingly, being comparable to the GNR width. This suggests that our SANTA technique could be extended to 2D materials such as graphene and transition metal dichalcogenides (TMDs) for patterning, functionalization, and sensor applications. Recent studies have shown up to 300 μA/μm current density in MoS_2 [34], yielding a power density per unit area P_A ~ 20 mW/μm² which is sufficient to remove the PMMA (Fig. 5).

Finally, we plot all our experimental results (CNTs and GNRs) for T_0 = 300 K, t_{PMMA} = 40 nm, t_{ox} = 90 nm in Fig. 6. The horizontal axis is the power density per unit area of contact with the substrate (P_A) and the vertical axis is the nanotrench width W normalized by the width of the device under test (W_{DUT}) (i.e., the CNT diameter or GNR width). The dashed line shows a power-law fitted by the exponent ~0.943 (see inset), consistent with the sub-linear trend described earlier.

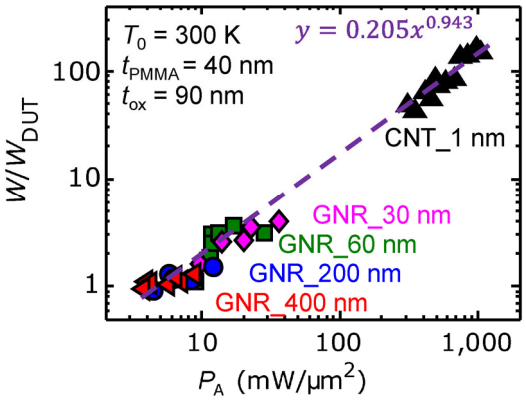

Figure 6 Nanotrench width normalized by the width of the device under test (i.e. GNR width or CNT diameter) as a function of input power (per unit area). Ambient temperature is 300 K, PMMA thickness is 40 nm and substrate is 90 nm SiO_2. Symbols are experimental results, the dashed line shows a power-law fitting with an exponent of 0.943, consistent with the sub-linear trend we observed between nanotrench width and input power.

3 Conclusions

In summary, we described the SANTA (self-aligned nanotrench ablation) technique, using Joule heating of a nanoscale heater (e.g. CNT or GNR) to create nanotrenches in PMMA along the direction of the underlying heater. These nanotrenches can be used to self-align materials or devices to be probed at ~10 nm scales using the CNT or GNR electrodes. We developed a 3D simulation model to understand and optimize the nanotrench formation process, showing that with lower ambient temperatures, thinner PMMA, and thinner substrate oxide, we gain better control over the nanotrench width. Guided by these simulations, we also experimentally demonstrated sub-20 nm nanotrenches at 150 K, using 30 nm PMMA film using CNT heaters. Sub-10 nm nanotrenches could be achieved by using thinner substrate oxide thicknesses for better vertical heat sinking. This technique could be extended to other nanoscale electrodes (e.g. nanowires or TMDs), providing a convenient way to position active materials with nanoscale precision. We demonstrated one potential application: building a nanoscale RRAM bit, self-aligned with a built-in CNT series resistor and selection device. Other applications include fabricating dielectric or metallic nanowires, selectively functionalizing sensors, facilitating catalytic nanowire growth, and removing undesired CNT connections.

Acknowledgements

We thank Dr. Eilam Yalon and Dr. Ilya Karpov for technical support and helpful discussions. We acknowledge partial support from the National Science Foundation (NSF) CAREER grant 1430530, SRC/Intel grant 2014-IN-2532, the Stanford SystemX Alliance, and the Stanford Nano- and Quantum Science and Engineering (NQSE) Postdoctoral Fellowship (F. X.).

Electronic Supplementary Material: Supplementary material (PMMA thickness calibration, devices on quartz substrates, and time-dependent study) is available in the online version of this article at http://dx.doi.org/10.1007/s12274-016-1180-0.

References

[1] Hochbaum, A. I.; Chen, R. K.; Delgado, R. D.; Liang, W. J.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. D.

Enhanced thermoelectric performance of rough silicon nanowires. *Nature* **2008**, *451*, 163–167.

[2] Yao, J.; Yan, H.; Lieber, C. M. A nanoscale combing technique for the large-scale assembly of highly aligned nanowires. *Nat. Nanotechnol.* **2013**, *8*, 329–335.

[3] Shulaker, M. M.; Hills, G.; Patil, N.; Wei, H.; Chen, H. Y.; Wong, H. S. P.; Mitra, S. Carbon nanotube computer. *Nature* **2013**, *501*, 526–530.

[4] Franklin, A. D.; Chen, Z. H. Length scaling of carbon nanotube transistors. *Nat. Nanotechnol.* **2010**, *5*, 858–862.

[5] Li, X. L.; Wang, X. R.; Zhang, L.; Lee, S. W.; Dai, H. J. Chemically derived, ultrasmooth graphene nanoribbon semiconductors. *Science* **2008**, *319*, 1229–1232.

[6] Schwierz, F. Graphene transistors. *Nat. Nanotechnol.* **2010**, *5*, 487–496.

[7] Bae, M. H.; Li, Z. Y.; Aksamija, Z.; Martin, P. N.; Xiong, F.; Ong, Z. Y.; Knezevic, I.; Pop, E. Ballistic to diffusive crossover of heat flow in graphene ribbons. *Nat. Commun.* **2013**, *4*, 1734–1740.

[8] Behnam, A.; Lyons, A. S.; Bae, M. H.; Chow, E. K.; Islam, S.; Neumann, C. M.; Pop, E. Transport in nanoribbon interconnects obtained from graphene grown by chemical vapor deposition. *Nano Lett.* **2012**, *12*, 4424–4430.

[9] Guo, X. F.; Small, J. P.; Klare, J. E.; Wang, Y. L.; Purewal, M. S.; Tam, I. W.; Hong, B. H.; Caldwell, R.; Huang, L. M.; O'Brien, S. et al. Covalently bridging gaps in single-walled carbon nanotubes with conducting molecules. *Science* **2006**, *311*, 356–359.

[10] Prasongkit, J.; Grigoriev, A.; Pathak, B.; Ahuja, R.; Scheicher, R. H. Transverse conductance of DNA nucleotides in a graphene nanogap from first principles. *Nano Lett.* **2011**, *11*, 1941–1945.

[11] Xiong, F.; Liao, A. D.; Estrada, D.; Pop, E. Low-power switching of phase-change materials with carbon nanotube electrodes. *Science* **2011**, *332*, 568–570.

[12] Xiong, F.; Bae, M. H.; Dai, Y.; Liao, A. D.; Behnam, A.; Carrion, E. A.; Hong, S.; Ielmini, D.; Pop, E. Self-aligned nanotube-nanowire phase change memory. *Nano Lett.* **2013**, *13*, 464–469.

[13] Kim, I. D.; Rothschild, A.; Tuller, H. L. Advances and new directions in gas-sensing devices. *Acta Mater.* **2013**, *61*, 974–1000.

[14] Kucsko, G.; Maurer, P. C.; Yao, N. Y.; Kubo, M.; Noh, H. J.; Lo, P. K.; Park, H.; Lukin, M. D. Nanometre-scale thermometry in a living cell. *Nature* **2013**, *500*, 54–58.

[15] Yun, J.; Jin, C. Y.; Ahn, J. H.; Jeon, S.; Park, I. A self-heated silicon nanowire array: Selective surface modification with catalytic nanoparticles by nanoscale Joule heating and its gas sensing applications. *Nanoscale* **2013**, *5*, 6851–6856.

[16] Jin, S. H.; Dunham, S. N.; Song, J. Z.; Xie, X.; Kim, J. H.; Lu, C. F.; Islam, A.; Du, F.; Kim, J.; Felts, J. et al. Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes. *Nat. Nanotechnol.* **2013**, *8*, 347–355.

[17] Zhang, H. J.; Wong, C.-L.; Hao, Y. F.; Wang, R.; Liu, X. G.; Stellacci, F.; Thong, J. T. L. Self-aligned nanolithography by selective polymer dissolution. *Nanoscale* **2010**, *2*, 2302–2306.

[18] Jin, C. Y.; Li, Z. Y.; Williams, R. S.; Lee, K. C.; Park, I. Localized temperature and chemical reaction control in nanoscale space by nanowire array. *Nano Lett.* **2011**, *11*, 4818–4825.

[19] Chen, C. C.; Lin, Y. S.; Sang, C. H.; Sheu, J. T. Localized joule heating as a mask-free technique for the local synthesis of ZnO nanowires on silicon nanodevices. *Nano Lett.* **2011**, *11*, 4736–4741.

[20] Englander, O.; Christensen, D.; Kim, J.; Lin, L. W. Post-processing techniques for locally self-assembled silicon nanowires. *Sensor. Actuat. A-Phys.* **2007**, *135*, 10–15.

[21] Liao, A.; Alizadegan, R.; Ong, Z. Y.; Dutta, S.; Xiong, F.; Hsia, K. J.; Pop, E. Thermal dissipation and variability in electrical breakdown of carbon nanotube devices. *Phys. Rev. B* **2010**, *82*, 205406.

[22] Xiong, F.; Liao, A.; Pop, E. Inducing chalcogenide phase change with ultra-narrow carbon nanotube heaters. *Appl. Phys. Lett.* **2009**, *95*, 243103.

[23] Shi, L.; Zhou, J. H.; Kim, P.; Bachtold, A.; Majumdar, A.; McEuen, P. L. Thermal probing of energy dissipation in current-carrying carbon nanotubes. *J. Appl. Phy.* **2009**, *105*, 104306.

[24] Salehi-Khojin, A.; Estrada, D.; Lin, K. Y.; Bae, M.-H.; Xiong, F.; Pop, E.; Masel, R. I. Polycrystalline graphene ribbons as chemiresistors. *Adv. Mater.* **2012**, *24*, 53–57.

[25] Li, Z. Y.; Bae, M. H.; Pop, E. Substrate-supported thermometry platform for nanomaterials like graphene, nanotubes, and nanowires. *Appl. Phys. Lett.* **2014**, *105*, 023107.

[26] Pop, E. The role of electrical and thermal contact resistance for Joule breakdown of single-wall carbon nanotubes. *Nanotechnology* **2008**, *19*, 295202.

[27] Pop, E. Energy dissipation and transport in nanoscale devices. *Nano Res.* **2010**, *3*, 147–169.

[28] Alizadegan, R.; Liao, A. D.; Xiong, F.; Pop, E.; Hsia, K. J. Effects of tip-nanotube interactions on atomic force microscopy imaging of carbon nanotubes. *Nano Res.* **2012**, *5*, 235–247.

[29] Lin, Y. C.; Bai, J. W.; Huang, Y. Self-aligned nano-lithography in a nanogap. *Nano Lett.* **2009**, *9*, 2234–2238.

[30] Hess, C.; Baumann, C.; Ammerahl, U.; Büchner, B.; Heidrich-Meisner, F.; Brenig, W.; Revcolevschi, A. Magnon heat transport in (Sr, Ca, La)$_{14}$Cu$_{24}$O$_{41}$. *Phys. Rev. B* **2001**, *64*, 184305.

[31] Islam, S.; Li, Z. Y.; Dorgan, V. E.; Bae, M. H.; Pop, E. Role of Joule heating on current saturation and transient behavior of graphene transistors. *IEEE Electr. Device L.* **2013**, *34*, 166–168.

[32] Pop, E.; Mann, D. A.; Goodson, K. E.; Dai, H. J. Electrical and thermal transport in metallic single-wall carbon nanotubes on insulating substrates. *J. Appl. Phys.* **2007**, *101*, 093710.

[33] Behnam, A.; Xiong, F.; Cappelli, A.; Wang, N. C.; Carrion, E. A.; Hong, S.; Dai, Y.; Lyons, A. S.; Chow, E. K.; Piccinini, E. et al. Nanoscale phase change memory with graphene ribbon electrodes. *Appl. Phys. Lett.* **2015**, *107*, 123508.

[34] English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett.* **2016**, *16*, 3824–3840.

Electronic Supplementary Material

SANTA: Self-aligned nanotrench ablation via Joule heating for probing sub-20 nm devices

Feng Xiong[1,†] (✉), Sanchit Deshmukh[1], Sungduk Hong[2], Yuan Dai[2], Ashkan Behnam[2], Feifei Lian[1], and Eric Pop[1] (✉)

[1] *Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA*
[2] *Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA*
[†] *Present address: Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, PA 15261, USA*

Supporting information to DOI 10.1007/s12274-016-1180-0

PMMA spin coating

We vary the PMMA thickness by controlling the spin rate (RPM) and the film composition—adding A-thinner to dilute the film.

Table S1 PMMA thickness achieved with different spin rates and compositions

Solution composition	RPM	Thickness (nm)
30% PMMA, 70% A-thinner	4,000	18
50% PMMA, 50% A-thinner	4,000	27
75% PMMA, 25% A-thinner	4,000	40
100% PMMA	6,000	45
100% PMMA	4,500	52
100% PMMA	3,500	57
100% PMMA	2,500	86
100% PMMA	1,500	113

Nanotrench at low temperature

The nanotrench width (W) is smaller at lower ambient temperature if all other conditions are the same. A comparison of two simulated nanotrench profiles at different ambient temperature (150 and 300 K, respectively) is shown in Fig. S2 below.

Address correspondence to Feng Xiong, fxiong@stanford.edu; Eric Pop, epop@stanford.edu

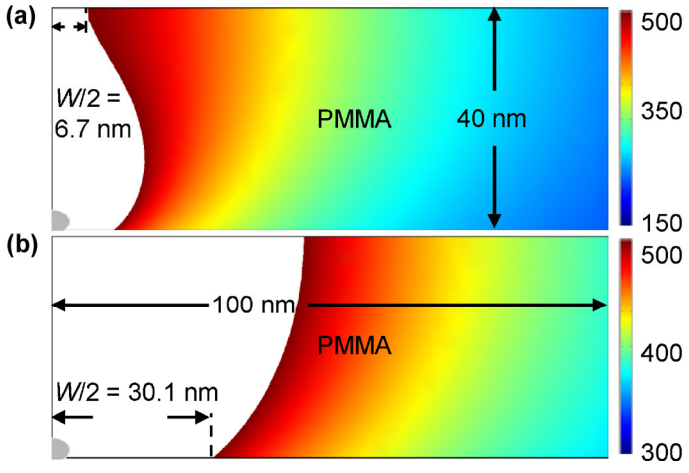

Figure S2 Nanotrench formed by CNT at different ambient temperatures. (a) T_0 =150 K. (b) T_0 = 300 K. The PMMA thickness is 40 nm and the substrate is 90 nm SiO_2 on a Si wafer (not shown).

Quartz substrate

We notice that if we perform trench formation simulations on quartz substrates, the trench width increases strongly (super-linearly) with the input power. We investigate this further with the FEM model. We build a model with the full thickness of the device (500 μm) instead of the reduced size (20 μm). We compare the substrate temperature profiles for devices on quartz and on 90 nm SiO_2 on Si in Fig. S3. We notice that due to the presence of the thermally resistive SiO_2 (k_{SiO_2} ~ 1.4 W/(m·K)) layer, the heating in the substrate is very localized (Fig. S3(a)). With the more thermally conductive quartz (k_{quartz} ~ 10 W/(m·K)) substrate, the entire substrate is being heated up (Fig. 3(b)). This heats up the PMMA film and creates much wider trenches.

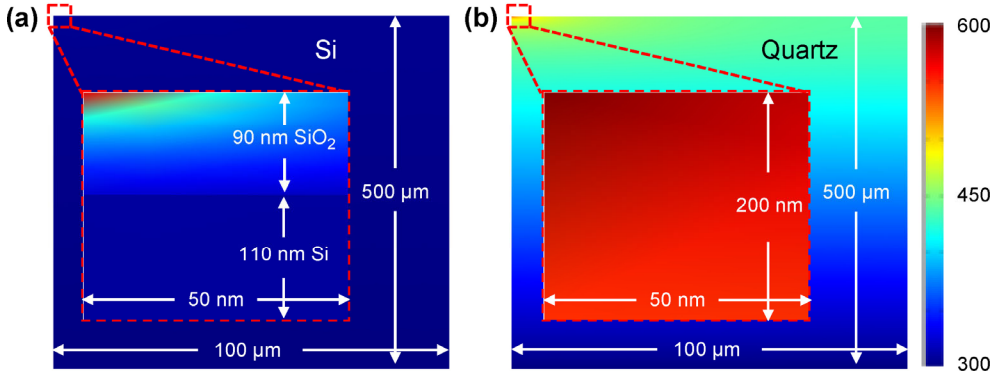

Figure S3 Substrate temperature profile when the CNT power is 0.5 mW/μm. PMMA thickness is 40 nm and ambient temperature is 300 K. The CNT is at the top left corner. (a) Substrate is 90 nm SiO_2 on 500 μm Si. (b) Substrate is 500 μm quartz. The higher thermal conductivity of quartz broadens the lateral temperature profile and significantly widens the PMMA trenches near the CNT.

Time dependence

In Fig. S4, we measure the nanotrench width formation using atomic force microscopy (AFM) as a function of time. The PMMA is 40 nm thick and ambient temperature is 300 K. The substrate is 90 nm SiO_2 on Si. After 1, 5 and 10 s the resulting nanotrench widths are 61, 80, 81 nm, respectively (at constant heating power of 0.31 mW/μm in the CNT). These time scales are much longer than the thermal time constant of the CNT + PMMA system (up to hundreds of nanoseconds [S1, S2]), suggesting that viscous flow plays a role in the trench formation process.

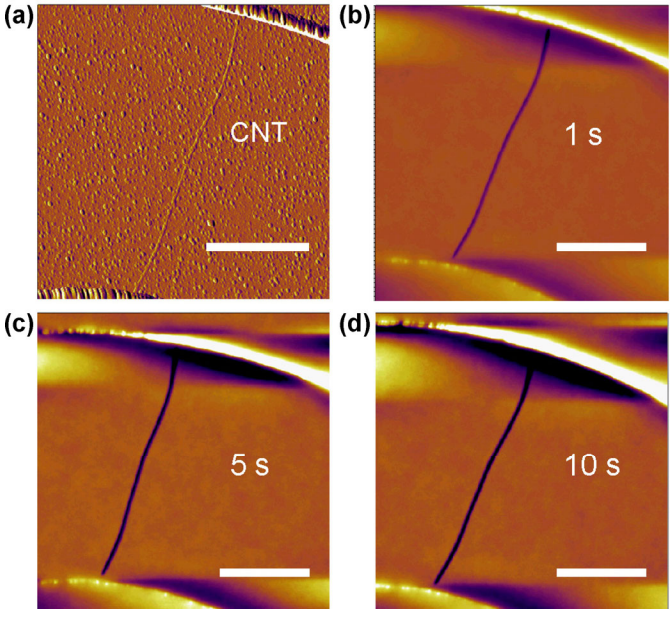

Figure S4 (a) AFM image of CNT on SiO_2 before coating with PMMA. (b)–(d) AFM images of nanotrench in PMMA after the CNT device is heated with 0.31 mW/μm for different time durations (1, 5 and 10 s) as listed. The metallic CNT has a length of 2.6 μm and a diameter of ~2 nm. Scale bars are 1 μm.

References

[S1] Pop, E. Energy dissipation and transport in nanoscale devices. *Nano Res.* **2010**, *3*, 147–169.

[S2] Islam, S.; Li, Z. Y.; Dorgan, V. E.; Bae, M. H.; Pop, E. Role of joule heating on current saturation and transient behavior of graphene transistors. *IEEE Electr. Device L.* **2013**, *34*, 166–168.