# Inducing chalcogenide phase change with ultra-narrow carbon nanotube heaters

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Carbon nanotube (CNT) heaters with sub-5 nm diameter induce highly localized phase change in $Ge_2Sb_2Te_5$ (GST) chalcogenide. A significant reduction in resistance of test structures is measured as the GST near the CNT heater crystallizes. Effective GST heating occurs at currents as low as 25 $\mu$A, significantly lower than in conventional phase change memory with metal electrodes (0.1–0.5 mA). Atomic force microscopy reveals nucleation sites associated with phase change in GST around the CNT heater. Finite element simulations confirm electrical characteristics consistent with the experiments, and reveal the current and phase distribution in GST. © *2009 American Institute of Physics*. [doi:10.1063/1.3273370]

Phase change memory (PCM) is a promising candidate for next-generation nonvolatile data storage,[1] combining features such as low operating voltage (~1 V), fast access times, high endurance, and potential for scaling below the size limits of Flash memory (~32 nm).[2] PCM devices rely on phase change materials like chalcogenides (e.g., $Ge_2Sb_2Te_5$ or GST) which exhibit sharply contrasting and switchable electrical resistivity and optical reflectivity[3] between their crystalline and amorphous states. PCM switching is induced through electrical (Joule) heating, which requires relatively high programming currents (0.1–0.5 mA) even when nanoscale heaters[2,4] or GST nanowires[5] are used. Reducing this programming current is one of the most significant challenges associated with PCM today.

In this study, we have successfully used individual carbon nanotubes (CNTs) as nanoscale heaters to induce ultra-narrow phase change regions in GST, while applying currents on the order of 10 $\mu$A. We found that GST sputtering is compatible with CNT devices, with conformal deposition and little apparent damage to the CNT. The low currents needed to induce phase change are a result of the excellent thermal stability (up to >1000 °C) and extremely small diameter (<5 nm) of the CNT heaters. We have also performed atomic force microscopy (AFM) imaging to examine the phase-change regions, and implemented a three-dimensional (3D) finite-element (FE) model to understand the resistive changes observed experimentally.

CNT devices used in this work are grown directly on $SiO_2$ and contacted with Pd electrodes as described in Refs. 6 and 7. We obtain both single-wall and small diameter (<5 nm) multiwall CNTs, and we find both can be used to induce phase change in GST. A 10 nm amorphous film of $Ge_2Sb_2Te_5$ (GST) was sputtered on top of the CNT devices, as shown in Fig. 1(a). Atomic force microscope (AFM) measurements confirm the thin GST was conformal, and surface roughness was minimally increased from ~0.3 nm (bare $SiO_2$) to ~0.5 nm (after GST deposition), as shown in Fig. S1 of Ref. 7. Moreover, electrical measurements of the CNT before and immediately after GST sputtering [Fig. 1(b)] indicate only ~20% change in CNT resistance, suggesting little damage to the nanotube from the sputtering process.

After GST sputtering we performed several compliance-limited dc current sweeps, while monitoring the voltage across the device, as shown in Fig. 2. Although the thin GST film spans between the two electrodes, its amorphous resistivity is very high (~100 $\Omega\cdot$cm), and the current is entirely carried by the CNT during the initial sweep (label no. 1). Subsequent sweeps to higher currents (no. 2–no. 6) lead to increasing conductivity with voltage snapback, attributed to a gradual transition of the GST surrounding the CNT from amorphous to crystalline phase. At higher currents the temperature of the CNT increases significantly,[8] and a low-resistance crystalline GST "sleeve" begins to form around the CNT. Once the phase transition occurs, the crystalline state of GST is preserved as seen from hysteresis loops in Fig. 2(a), with each forward sweep following the previous backward sweep (e.g., reverse and forward arrows between no. 2 and no. 3, respectively). Sweeps labeled no. 1–no. 6 were made by gradually increasing the upper current limit in 20 $\mu$A increments. Consequently, the resistance of the CNT-GST structure is reduced by more than an order of magnitude, as an increasing volume of GST surrounding the CNT gradually heats up and crystallizes, introducing a parallel current flow path. Once the current reached ~160 $\mu$A (sweep no. 7) the GST was irreversibly damaged, but the

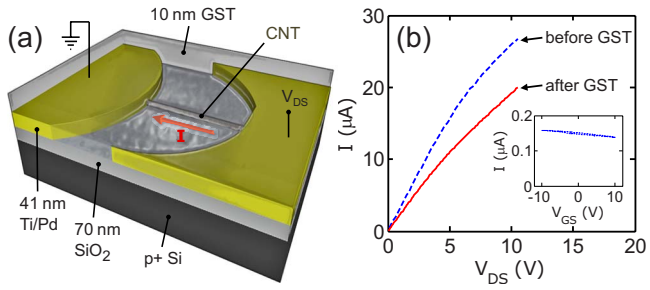


FIG. 1. (Color online) (a) Schematic of CNT test structure with GST thin film sputtered on top. (b) Measured current-voltage of a typical CNT ($L \approx 1.88$ $\mu$m, $d \approx 3.3$ nm) before and after GST deposition. The inset displays the measured current vs back-gate voltage, indicating metallic behavior.

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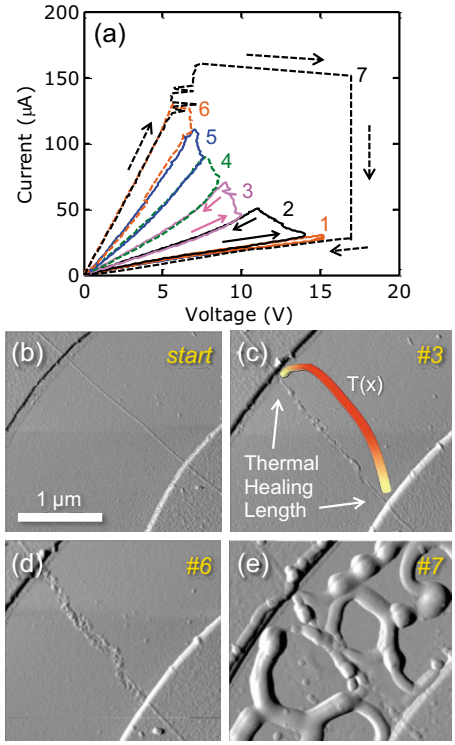


FIG. 2. (Color online) Measured and imaged phase change of GST covering CNT heater. (a) Consecutive current sweeps to progressively higher current. Each state is preserved when the GST is returned to zero current (room temperature). (b) Topographic AFM before any current is applied and [(c)–(e)] after current sweep to ~70, 130, and 160 $\mu$A, respectively. The latter correspond to traces no. 3, 6, and 7 labeled in (a). As current passes through the device, the CNT heats up and crystallizes the surrounding GST. In (c), the color profile shows the qualitative Joule heating temperature rise of the CNT, e.g., see Refs. 8 and 9. The GST near the middle of the CNT is crystallized first, illustrating the role of heat sinking at the CNT contacts (thermal healing length ~0.25 $\mu$m). At higher currents the GST covering the entire CNT is crystallized as shown in (d), and eventually fails (e).

measured $I-V$ returned along the original path (no. 1), indicating the CNT itself was still conducting, unchanged, and undamaged. The last point highlights the resilience of CNTs even under the most extreme conditions, and their durability as nanoscale GST heaters. We note the heating current at which GST phase transition first occurs (~25 $\mu$A) is much lower than in conventional PCM, although voltages are higher due to the relatively long, resistive CNT (~400 kΩ). Shorter CNTs (<1 $\mu$m) with good contacts have resistance an order of magnitude lower,[10] and would yield effective heating at voltages that are proportionally decreased as well.[8]

AFM images in Figs. 2(b)–2(e) were taken after sweeps no. 1, 3, 6, and 7, respectively, showing the progression of the GST surface as the structure is pushed to higher currents. As the GST begins to crystallize, nucleation points form along the length of the heated CNT, consistent with observations in GST nanowires.[11] These nucleation centers eventually lead to GST volume changes, possible void formation (likely due to thermal expansion mismatch)[12] and delamination from the CNT as the height profile increases up to ~7 nm. The region of nucleation follows the well-known Joule heating temperature profile of a CNT on $SiO_2$.[8,9] In fact, Fig. 2(c) reveals that phase and volume changes in GST occur initially near the middle of the CNT, where the temperature is highest. This leads to a "visualization" of the thermal healing length ($L_H \sim 0.25$ $\mu$m) along the CNT, i.e., the length scale over which heat sinking from the metal contacts remains effective.[8,9] At distances greater than $L_H$ from the contacts, the CNT heat sinking is limited by the $SiO_2$ substrate. Eventually the entire GST around the CNT heats up and crystallizes [Fig. 2(d)], leading to the large measured increase in conductance. The GST breakdown electrically observed at ~160 $\mu$A appears as a physical "bubbling" and delamination of the thin film [Fig. 2(e)].

To better understand the heating and crystallization in this test structure, we implemented a 3D finite element (FE) model[13] that self-consistently takes into account the electrical, thermal, and Joule heating interactions. The simulated structure shown in Fig. 3(a) mimics that of the experimental devices (Figs. 1 and 2). In the electrical model, the Poisson and continuity equations are solved to obtain the voltage and current distribution in the device. Simulation parameters are similar to Ref. 14 and summarized in Ref. 7. In addition, the electrical[15] and thermal conductivity[16] of GST ($\sigma_{GST}$ and $k_{GST}$) are parameterized as a function of phase and temperature, as shown in Ref. 7. The transition temperatures are taken as those well-known for GST, i.e., 150 °C for the amorphous to fcc transition (~1000×$\sigma_{GST}$ increase), and 350 °C for the fcc to hcp transition (additional ~10×$\sigma_{GST}$ increase).

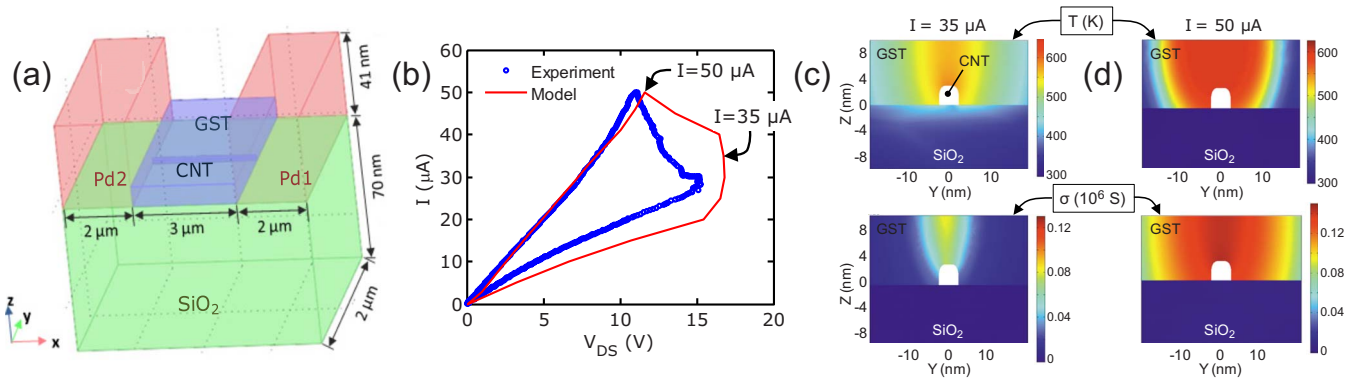


FIG. 3. (Color online) Simulation of GST heating and phase change with CNT heater. (a) Device structure used in the 3D simulation mimics the experimental test structures. (b) Measured (symbols) and simulated (lines) $I-V$ characteristics of a typical metallic CNT covered by GST. The FE model predicts a sudden increase in overall conductivity as the GST changes to hcp crystalline state. [(c) and (d)] Cross-sectional temperature (top) and conductivity (bottom) of GST at the middle of the CNT at $I$=35 and 50 $\mu$A, respectively. The simulations suggest that noticeable voltage snapback only occurs when ~5–10 nm of GST near the CNT transitions to hcp phase.

The electrical conductivity and Joule heating of the CNT are calculated following Ref. 8, including the temperature- and position-dependent carrier mean free paths. On all external boundaries, electrical insulation boundary conditions apply, except across the electrodes where a constant current flow is applied. The heat diffusion equation is used to obtain the 3D temperature and phase distribution in the device. In other words, when the GST reaches a phase transition temperature, it is switched to the corresponding phase, which is then preserved upon return to room temperature (Fig. S2 in Ref. 7).

Adiabatic thermal boundary conditions are used on all exterior boundaries (convective air cooling and radiation loss are insignificant) except for the bottom boundary of the $SiO_2/Si$ interface, where a constant temperature 300 K is assumed. At interior boundaries, thermal boundary resistance (TBR, $R_{th}$) is used to model the heat fluxes and temperature gradients at the interfaces.[17] The TBR is included by adding a thin thermally resistive layer with thickness $d_{th}$ and thermal conductivity $k_{th}$ such that $R_{th}=d_{th}/k_{th}$. The Pd/CNT boundary is assumed to have $R_{th,c}=1.2\times10^{7}$ K/W, and a thermal boundary conductance $g=0.17$ W/K/m per CNT length is applied at the CNT/$SiO_2$ boundary.[8,18] All other interior boundaries have $R_{th}=2.5\times10^{-8}$ $m^2$ K/W per unit area, and all TBR is assumed to be temperature independent.[14,17]

Figure 3(b) displays typical current-voltage characteristics computed with this model (line), compared to experimental data (circles) for a typical CNT/GST device with $L\approx3$ $\mu$m, and $d=3.2$ nm. The simulation performs current sweeps while monitoring the voltage, as does the experimental data. No changes are noted in the simulated $I-V$ characteristics as the GST warms up beyond ~150 °C and changes into fcc crystalline state. At $I\approx30$ $\mu$A the temperature in the GST surrounding the CNT heater reaches ~350 °C, the transition temperature of GST from fcc to hcp state. As more GST switches to the highly conductive hcp state, the resistance of the device begins to decrease significantly, with a parallel current path being created in the GST. Hence, the voltage decreases even as the current increases. Figures 3(c) and 3(d) show Y-Z plane cross-sections of temperature and electrical conductivity in GST at the center of the CNT before and after the voltage snapback seen in the simulated device $I-V$ curve. At $I=35$ $\mu$A the GST directly above the CNT heater has partially switched to the highly conductive hcp state. At $I=50$ $\mu$A, a significant amount of GST near the CNT was transformed into the hcp state. A parallel current path is now available in GST which causes the voltage snapback shown in Fig. 3(b).

In the backward sweep, the hcp state of GST is preserved upon return to room temperature, and the $I-V$ curve follows a lower resistance path. Thus, interestingly, the simulations indicate that voltage snapback in this test structure is due to the fcc to hcp transition of GST, not the amorphous to fcc transition. This occurs although the resistance of GST decreases by three orders of magnitude in the fcc phase (from gigaohm to megaohm range), the total resistance of the entire device is still dominated by the CNT (~0.1 MΩ). Only a transition to the hcp state brings the GST "sleeve" surrounding the CNT into a resistance range comparable to that of the CNT, leading to a measurable change in the electrical characteristics (Figs. 2 and 3). As heating to the hcp phase is easily reached, the CNT heater can also be used to melt the GST,[19] although an optimized test structure should be employed to achieve fast (~nanoseconds) quenching into the amorphous phase.

In conclusion, we have demonstrated that CNT heaters with sub-5 nm diameters can induce highly localized phase change in GST thin films, with heating currents of the order ~25 $\mu$A. The current-voltage characteristics of simple test devices show voltage snapback behavior, indicating GST switching from highly resistive (amorphous) to highly conductive (hcp crystalline) states. Additional AFM characterization and 3D FE modeling confirm the morphological and phase changes occurring. The simulation platform can also be used for future studies, to provide insight into optimized, lower current, and reversible switching device structures. This proof-of-concept study opens up the possibility of developing phase-change memory cells with CNT heaters and ultra-low switching energy.

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[19] Probably in part responsible for the delamination of the GST at high power in Fig. 2(e).

**Supporting Online Materials** for "*Inducing Chalcogenide Phase Change with Ultra-Narrow Carbon Nanotube Heaters*" by F. Xiong, A. Liao, E. Pop, Univ. Illinois Urbana-Champaign

**1. Methods of CNT Fabrication:** Carbon nanotubes (CNTs) were grown by chemical vapor deposition using a mixture of $CH_4$ and $C_2H_4$ as the carbon feedstock, and $H_2$ as the carrier gas at 900 $^oC$. The flow rate of $CH_4$ to $C_2H_4$ was kept large to grow predominantly single-walled CNTs. Fe (~2 Å thick deposited by e-beam evaporation) is used as the catalyst for CNT growth. The catalyst was deposited on ~100 nm thick $SiO_2$ and highly p-doped Si wafers. Patterned catalyst islands are formed using photolithography and lift-off. Prior to growth, catalysts were annealed at 900 $^oC$ in Ar environment to ensure the formation of Fe nanoparticles, from which the CNTs grow. The nanotubes were contacted with Ti/Pd (1/40 nm) electrodes defined using photolithography. The electrode separation on our test chips is varied from L ~ 1-10 μm.

**2. GST Thin Film Deposition:** GST thin film deposition is done in high vacuum using *ATC 2000* custom four gun co-sputtering system (AJA International), with a deposition rate at 0.4 Å/s. Deposition at this rate ensures that there is only minimal damage to the CNT from the sputtering process. The sputtering target $Ge_2Sb_2Te_5$ was purchased from *ACI Alloys Incorporate*. Thin film thickness is characterized with X-ray reflectivity measurement using *Philips Xpert Pro XRD* system on control samples. By probing diffraction intensities at glancing angles of incidence, we are able to confirm the GST thin film thickness is 10.0 nm ± 0.4 nm (Fig. S1a).

We have also performed atomic force microscopy (AFM) measurement on our samples before and after GST deposition (Fig. S1b and S1c, respectively). The measured surface roughness of our devices only increased minimally from 0.3 nm to 0.5 nm.

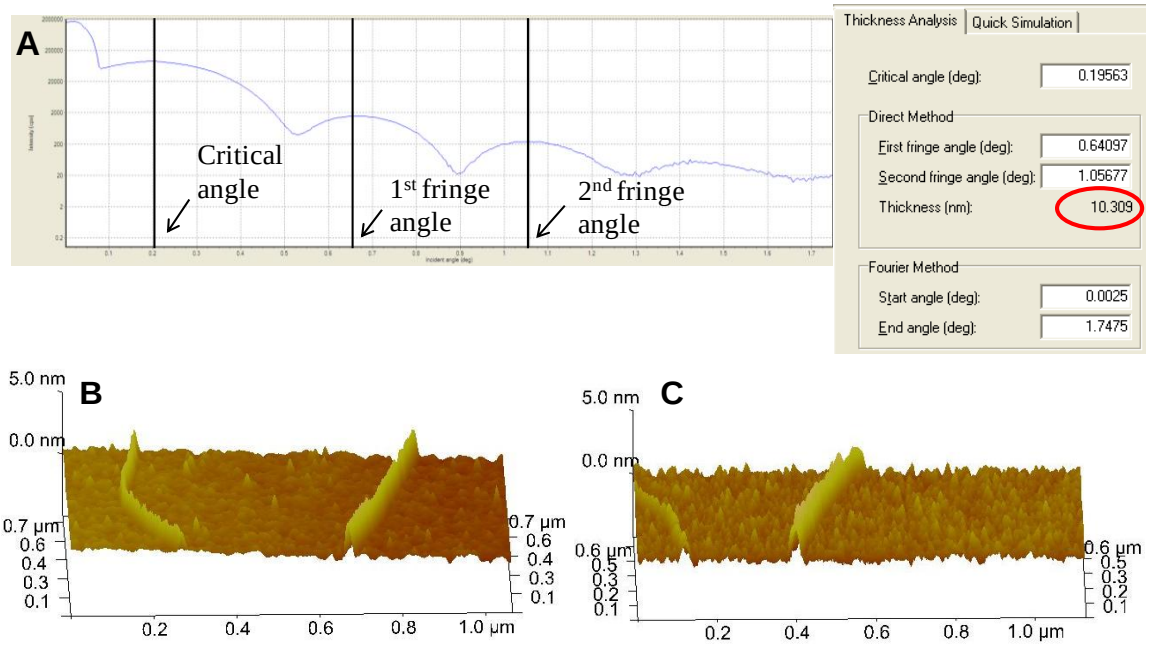


***FIG. S1. (A)*** *X-ray reflectivity measurement of the sputtered GST thin film using control samples. The control sample is fabricated by sputtering GST directly onto highly doped Si substrate immediately after the removal of the native oxide layer by wet etching. The measurement confirms the GST thin film thickness is 10 nm.* ***(B)*** *and* ***(C)*** *AFM images of a CNT before and after GST deposition indicating the depositted GST thin film is conformal.*

**3. Finite Element Modeling Parameters:** The electrical resistivity and thermal conductivity of GST are parameterized as a function of their crystalline state and the temperature using known experimental results, as shown in Fig. S2.

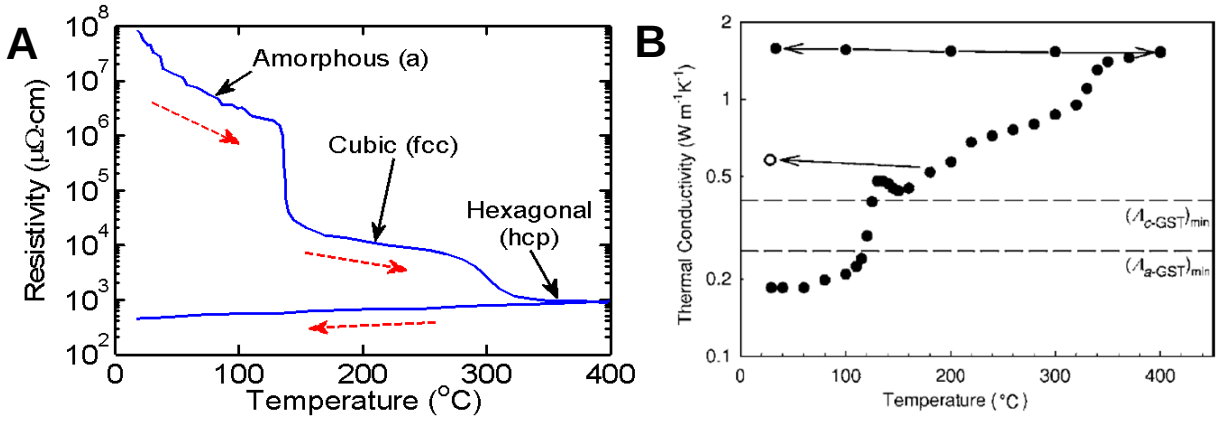


***FIG. S2. (A)*** *Temperature dependence of GST electrical resistivity* $\sigma_{GST}(T)$.[1] ***(B)*** *Temperature dependence of GST thermal conductivity* $k_{GST}(T)$.[2]

The table below summarizes the thermal and electrical properties used for the Finite Element (FE) simulation in this paper:

| | **k (W/m/K)** | **C (J/m$^3$/K)** | **σ (S/m)** |
|---|---|---|---|
| **Pd** | 22 | 2.93 x $10^6$ | 1 x $10^7$ |
| **$SiO_2$** | 1.4 | 1.72 x $10^6$ | 1 x $10^{-16}$ |
| **GST** | $k_{GST}(T)$ | 1.24 x $10^6$ | $\sigma_{GST}(T)$ |
| **CNT** | 3000 | 1.10 x $10^6$ | $\sigma_{CNT}(T)$ |

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