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Research Article

Toward Low-Temperature Solid-Source Synthesis of Monolayer MoS_2

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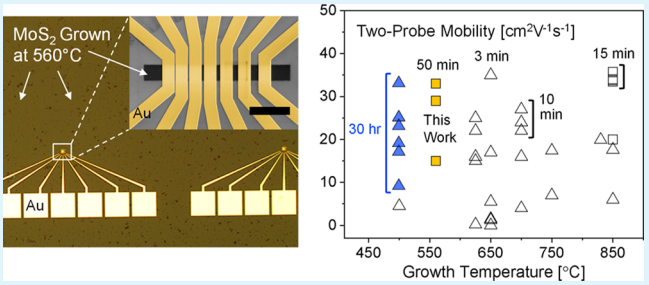
ABSTRACT: Two-dimensional (2D) semiconductors have been proposed for heterogeneous integration with existing silicon technology; however, their chemical vapor deposition (CVD) growth temperatures are often too high. Here, we demonstrate direct CVD solid-source precursor synthesis of continuous monolayer (1L) MoS_2 films at 560 °C in 50 min, within the 450-to-600 °C, 2 h thermal budget window required for back-end-of-the-line compatibility with modern silicon technology. Transistor measurements reveal on-state current up to ~140 μA/μm at 1 V drain-to-source voltage for 100 nm channel lengths, the highest reported to date for 1L MoS_2 grown below 600 °C using solid-source precursors. The effective mobility from transfer length method test structures is 29 ± 5 cm^2 V^{-1} s^{-1} at 6.1 × 10^{12} cm^{-2} electron density, which is comparable to mobilities reported from films grown at higher temperatures. The results of this work provide a path toward the realization of high-quality, thermal-budget-compatible 2D semiconductors for heterogeneous integration with silicon manufacturing.



KEYWORDS: *2D materials, transition metal dichalcogenides, MoS_2, molybdenum disulfide, BEOL, back-end-of-the-line, chemical vapor deposition, CVD growth, carrier mobility*

INTRODUCTION

Since the era of the first integrated circuits, improving semiconductor device density has continuously translated into benefits for more advanced computing systems.[1] The horizontally stacked gate-all-around nanosheet transistor with 3 nm thick Si nanosheets is expected to replace the FinFET structure to continue transistor scaling beyond the 5 nm technology node.[2] However, further gate length scaling or better control over off-state leakage requires thinner body channel materials,[3] making atomically thin two-dimensional (2D) materials extremely appealing for use in next-generation computing devices. While graphene, the first 2D material discovered, is a semimetal with 0 eV band gap,[4] a class of 2D layered materials known as transition-metal dichalcogenides (TMDs) have band gaps ranging from semimetallic (0 eV) to semiconducting (~2.5 eV) energies.[5,6] TMDs retain sizable band gaps and carrier mobilities down to monolayer thicknesses[7] less than 1 nm, whereas Si thinned below ~4 nm faces severe mobility degradation issues due to surface roughness fluctuations.[8−10]

Specifically, MoS_2 has become one of the most promising TMDs due to its band gap (~2.2 eV for monolayer MoS_2[11,12]) and controllable growth of consistent large-area MoS_2 films down to monolayer (1L) thicknesses, making MoS_2 a viable candidate for large-scale semiconductor applications.[13−18] Although moving MoS_2 away from tedious and inconsistent mechanical exfoliation techniques has enabled systematic studies for electronics applications,[16,19,20] the quality of synthesized MoS_2 has not always been ideal, especially from the standpoint of the device fabrication thermal budget. If MoS_2 is to be integrated in the back end (i.e., after silicon) of modern integrated circuits, the fabrication process of as-grown MoS_2 transistors cannot exceed the range of 450−600 °C (depending on the process time) for integration with logic applications,[21−24] although some three-dimensional (3D) vertical memory applications can withstand >700 °C.[25] For example, irreversible degradation of certain silicide contacts, interlayer dielectrics, and diffusion barrier layers have been observed with thermal budgets over 600 °C for 2 h.[21,26,27]

In this work, we report direct chemical vapor deposition (CVD) growth of continuous monolayer MoS_2 films using solid-source precursors at 560 °C in 50 min, within the thermal budget of modern integrated circuit processing. Comparing the

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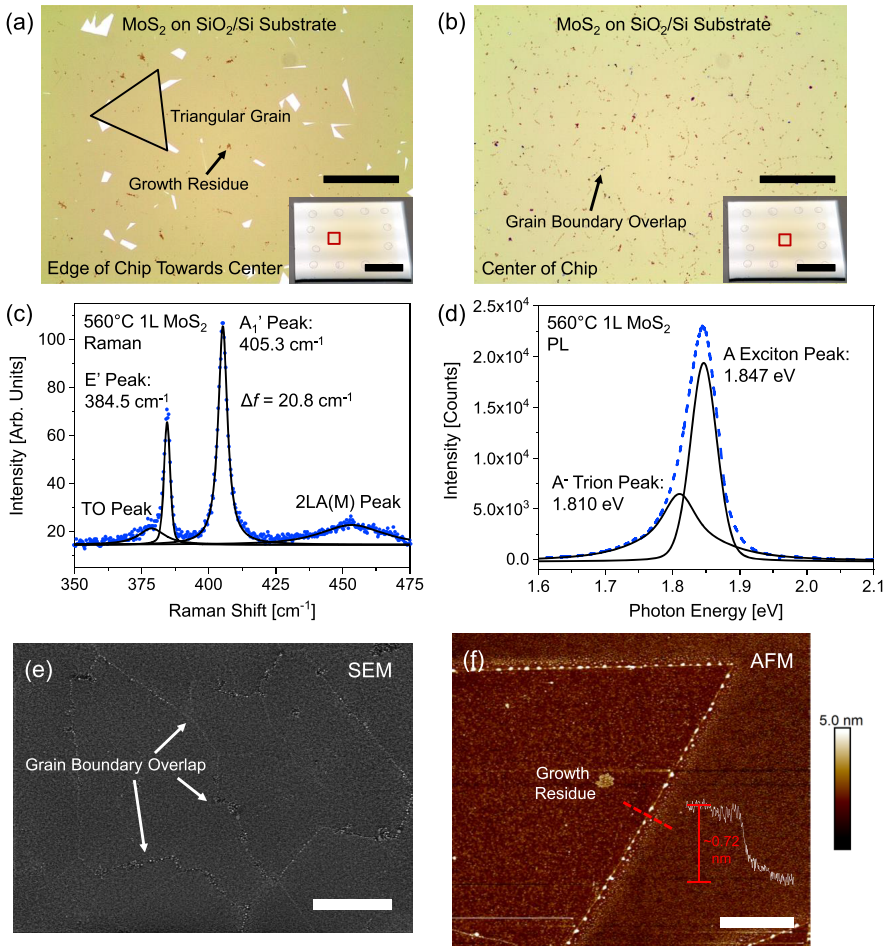

Figure 1. Monolayer MoS_2 grown at 560 °C. (a,b) Optical images of monolayer (1L) MoS_2 grown by CVD at 560 °C on SiO_2/Si at (a) 7 mm from the edge of the substrate and (b) the center of the substrate. Larger ~60 μm triangular grains are seen 7 mm from the edge, which merge into a continuous film with overlapping grain boundaries at the center. Scale bars are 20 μm. Insets show the 1.5 × 2 cm substrates, with red boxes marking the location of the optical images. Circles are "coffee rings" corresponding to the PTAS droplets. Inset scale bars are 7 mm. (c) Raman spectrum of 1L MoS_2 grown at 560 °C on SiO_2/Si (blue dots). Pseudo-Voigt curves (black lines) fit the E′ mode at 384.5 cm^{-1} and the A_1' mode at 405.3 cm^{-1} with a peak separation Δf = 20.8 cm^{-1}. The longitudinal acoustic 2LA(M) peak is centered at 453.3 cm^{-1}, and the TO shoulder peak is centered at 378.8 cm^{-1}. (d) PL spectrum of the same 1L MoS_2 (blue dashed line). Pseudo-Voigt curves (black lines) fit the A exciton peak at 1.847 eV and the charged A^- trion peak at 1.810 eV. A laser with an excitation wavelength of 532 nm was used for all measurements. (e) SEM of the continuous 1L MoS_2 film at the center of the substrate with overlapping grain boundaries. Scale bar is 3 μm. (f) AFM of 1L MoS_2 triangular grains on SiO_2/Si away from the substrate center. MoS_2 appears ~0.72 nm thick from the step height, in close agreement with the accepted monolayer MoS_2 thickness (0.615 nm).[56] Growth residue (most likely caused by excess partially reduced MoO_3 precursor) is observed on the MoS_2 grains and along the grain edges. Scale bar is 2 μm. Both SEM and AFM indicate that 1L MoS_2 is grown without bilayer (2L) MoS_2 nucleation.

metrics of the I_{on}/I_{off} current ratio, drive current, contact resistance, and carrier mobility, transistors made from these as-grown films show performance levels similar to those reported for monolayer MoS_2 grown at higher temperatures.[13,16,28−34] This work provides a path toward the realization of high-quality, thermal-budget-compatible TMD materials, which could further improve future computing and data storage.

GROWTH AND MATERIAL CHARACTERIZATION

The thermal budget for modern silicon integrated circuit processing dictates that fabrication of BEOL (back-end-of-the-line) devices and materials cannot exceed 550 °C for 2 h,[26,27] and stricter temperature budgets are needed if process times are longer. This limitation is imposed by gate work function instability and silicide contact degradation.[27] Certain interlayer low-κ dielectrics (e.g., SiCOH) could require even lower thermal budgets, below 450 °C for 2 h,[21] although SiCOH integrity could be maintained up to 525 °C for 2 h using some BEOL processes.[24] Thus, in order to incorporate new materials such as MoS_2 into stacked, heterogeneous integrated circuits that increase the transistor density in the third dimension,[35] their BEOL thermal budget becomes crucial. However, direct monolayer (1L) MoS_2 growths with good electrical properties have typically been obtained using solid-source precursor CVD above 650 °C.[13,16,28−34] Wafer-scale 1L MoS_2 grown using metal−organic CVD (MOCVD)[14,36−41] at or below 500 °C appears within the BEOL temperature budget, but the growth times have been >8 h, which limit throughput, and the average carrier mobilities reported remain lower than the best MoS_2 grown at higher temperatures. Efforts to develop atomic layer deposition of MoS_2 at temperatures as low as 50 °C are also underway,[42,43] but the resulting films are amorphous and require post-growth anneals above 800 °C to improve their crystallinity.[44−46]

Here, we grew continuous 1L MoS_2 films at 560 °C in 50 min using solid sulfur (S) and molybdenum trioxide (MoO_3)

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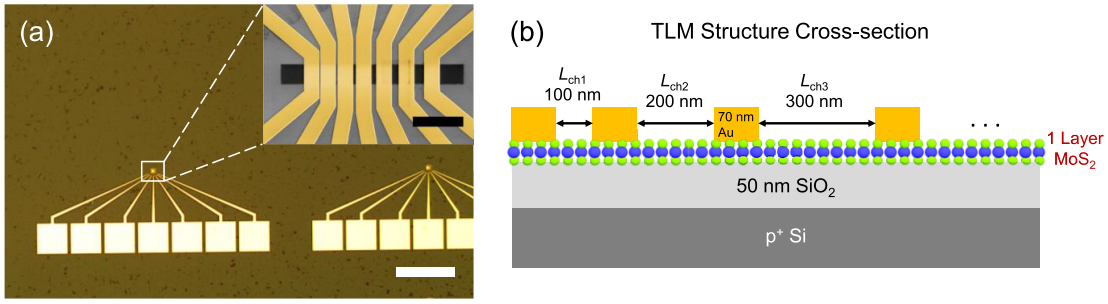

Figure 2. TLM structures. (a) Optical image of the TLM structures with channels ranging from L_{ch} = 100 to 700 nm. The large, square probe pads (20 nm SiO_2/2 nm Ti/40 nm Au) lead into fine contacts (70 nm Au). Scale bar is 100 μm. Inset: enlarged, colorized SEM of the fine leads directly contacting the monolayer MoS_2 channel. The channel was etched 18 μm long × 2 μm wide (darker region) after the contact metal deposition. Inset scale bar is 5 μm. (b) Cross-section schematic of the TLM test structure. The gold contact lengths are 1.5 μm wide (not to scale). The Si substrate serves as the gate (G), and pairs of Au contacts serve as the drain (D) and grounded source (S) in subsequent measurements.

precursors with the aid of perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS).[13,15,17,18] PTAS dissolved in water is deposited as droplets around the perimeter of 1.5 × 2 cm chips with thermally grown SiO_2 on p^+ silicon, which also serves as the back-gate for field-effect transistors (FETs).[13] The PTAS droplets dry up into "coffee rings" around the perimeter of the substrate before the seeded SiO_2/Si chips are placed face down on top of an alumina (Al_2O_3) crucible containing MoO_3 powder. Trace amounts of PTAS diffuse from the dried "coffee rings" toward the center of the chip to facilitate MoS_2 nucleation during growth. Excess solid sulfur source melted in a quartz boat is placed at an optimal position upstream near the incoming Ar gas flow inlet, all enclosed within a cylindrical quartz tube.

In addition to the PTAS seed layer promoting initial MoS_2 nucleation from which grains grow, the trace amounts of carbon from the diffusing seed layer also act as a catalyst, promoting reduction of MoO_3 powder into volatile suboxide MoO_{3-x}.[47] The reduction of MoO_3 into MoO_{3-x} is crucial for incoming S to react with volatile molybdenum (Mo) species in order to grow MoS_2. It is important to note that at growth temperatures around 560 °C, MoO_3 reduction is near the limit of reaction with trace amounts of carbon present.[47] Both the reduced system pressure of 490 Torr and the incoming volatile sulfur introduced at elevated temperatures promote the reduction of MoO_3 into volatile suboxide MoO_{3-x}.[48] When sufficient volatile MoO_{3-x} is matched with an optimal flux of incoming sulfur atoms on the substrate surface, further reaction occurs to grow 1L MoS_2 films. As shown in Figure 1a,b, relatively clean 1L MoS_2 films can be grown at 560 °C in 50 min on 1.5 × 2 cm chips. This is the lowest thermal budget that produced clean, sizable (>10 μm) MoS_2 triangular grains merged into a continuous film using solid source precursors in our system. Larger ~60 μm triangular grains are seen (a) 7 mm from the edge of the substrate, which merge into a continuous film with overlapping grain boundaries at (b) the center of the substrate.

Raman spectroscopy and photoluminescence (PL) are utilized to confirm that 1L MoS_2 is present from its characteristic phonon (lattice vibrations) and excitonic (electron−hole pair generation) properties, respectively. In order to ensure strong, well-defined detectable signals, all Raman and PL measurements were performed on 1L MoS_2 grown on 90 nm SiO_2/Si substrates using a green laser with excitation wavelength of 532 nm. Due to the Lorentzian nature of the Raman (and PL) peaks and the Gaussian nature of the laser spatial intensity, pseudo-Voigt curves were used to capture each peak fit.[49] Figure 1c shows the Raman spectrum of 1L MoS_2 grown at 560 °C (blue dots). Pseudo-Voigt curves (black lines) fit the Raman peaks of 1L MoS_2, namely, the in-plane E′ mode at 384.5 cm^{-1} and the out-of-plane A_1' mode at 405.3 cm^{-1} with a peak separation Δf = 20.8 cm^{-1}, which is characteristic of as-grown 1L MoS_2[13,50] with slight intrinsic tensile strain due to thermal coefficient of expansion mismatch between the 2D material and the underlying SiO_2 substrate.[51] Because odd-numbered, few-layer MoS_2 (including 1L MoS_2) belong to the D_{3h} point group, the two main Raman active modes are denoted E′ and A_1'.[13,52] The 2LA(M) peak is seen around 453.3 cm^{-1}, and the transverse optical (TO) shoulder peak is seen at 378.8 cm^{-1}.[53]

Characteristic PL measurements are shown in Figure 1d. We note that these probe the optical band gap of 1L MoS_2, which is smaller than the electronic gap of 1L MoS_2 by the exciton binding energy (0.2 to 0.6 eV),[11] and all three of these energies depend on the environmental dielectric screening.[54] Pseudo-Voigt curves (black lines) fit the PL spectrum, identifying the ground state A exciton at 1.847 eV and the charged A^- trion at 1.810 eV. (The A^- trion is a charged exciton with an extra electron coupled to the electron−hole pair.) We did not observe a B exciton in our samples (0.1 to 0.2 eV above the A peak), which has been used to assess nonradiative recombination, with low (or no) B peak suggesting higher sample quality.[55]

To further show that 1L MoS_2 is grown by CVD at 560 °C, scanning electron microscopy (SEM) is shown in Figure 1e of the continuous 1L MoS_2 film at the center of the substrate, with overlapping grain boundaries. Atomic force microscopy (AFM) of 1L MoS_2 triangular grains on SiO_2/Si, away from the substrate center, is also shown in Figure 1f. MoS_2 is measured to be ~0.72 nm thick from the step height, which is in good agreement with the accepted monolayer MoS_2 thickness (0.615 nm).[56] Growth residue (most likely caused by excess partially reduced MoO_3 precursor) is observed on the MoS_2 grains and along the grain edges. Both SEM and AFM indicate that 1L MoS_2 is grown without bilayer (2L) MoS_2 nucleation.

■ ELECTRICAL RESULTS AND DISCUSSION

Transfer length method (TLM) structures[57] were fabricated on 560 °C 1L MoS_2 as-grown on a 50 nm SiO_2 on p^+ Si substrate, which also serves as the back-gate for all devices. Figure 2a shows an optical image of the TLM structures as

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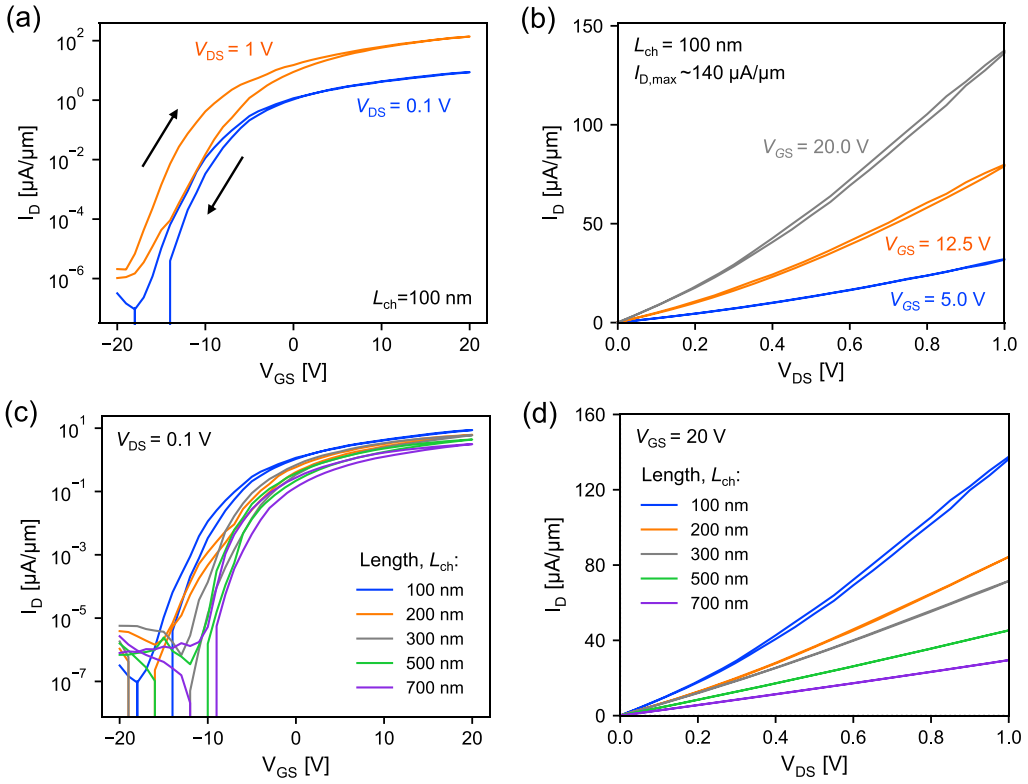

Figure 3. Electrical characteristics. Transistors fabricated using monolayer MoS_2 grown at 560 °C on SiO_2/Si substrates. (a) Measured I_D vs V_{GS} transfer curves at V_{DS} = 0.1 and 1 V for a 100 nm channel device (L_{ch} = 100 nm). The small arrows mark forward (left I_D branch) and backward (right I_D branch) voltage sweep directions, illustrating small hysteresis. A current ratio $I_{on}/I_{off} \sim 10^7$ is observed, and the SS is estimated to be SS ≈ 1150 mV/dec from the forward sweep at V_{DS} = 0.1 V. (b) Measured I_D vs V_{DS} curves at V_{GS} = 5 to 20 V for the same L_{ch} = 100 nm channel length device. The maximum drive current achieved was $I_{D,max} \sim 140\ \mu A/\mu m$ at V_{DS} = 1 V. Current saturation was not observed because the threshold voltage V_T keeps this device in the linear operating region throughout.[30] (c) Measured I_D vs V_{GS} transfer curves at V_{DS} = 0.1 V for transistors with channel lengths from L_{ch} = 100 to 700 nm. (d) Measured I_D vs V_{DS} at V_{GS} = 20 V for transistors with channel lengths from L_{ch} = 100 to 700 nm. I_D decreases for increasing channel lengths as expected due to the larger channel resistance. All device channels are 2 μm wide, and all measurements were performed at room temperature in a vacuum probe station. All electrical measurements shown are double sweeps (voltage swept up and down), revealing minimal hysteresis.

fabricated by electron-beam lithography. The large, square probe pads (20 nm SiO_2/2 nm Ti/40 nm Au) lead into the fine contacts (70 nm Au). The colorized SEM inset shows the pure Au leads directly contacting the monolayer MoS_2 channel, which was etched 18 μm long × 2 μm wide (darker region) after the contact metal deposition. Figure 2b shows the cross-section schematic of the TLM test structure with adjacent contact channel lengths ranging from L_{ch} = 100 to 700 nm, forming a series of back-gated FETs.

Figure 3a shows the measured drain current I_D (normalized by width) versus back-gate voltage V_{GS} transfer curves at drain voltages V_{DS} = 0.1 and 1 V for a 100 nm channel device (L_{ch} = 100 nm). The small arrows mark forward (left I_D branch) and backward (right I_D branch) voltage sweep directions, illustrating small hysteresis and charge trapping between MoS_2 and the back-gate SiO_2 dielectric. The maximum gate leakage observed was ~1 nA at V_{GS} = 20 V, which is 3−4 orders of magnitude smaller than the drain current in the on-state. A current ratio $I_{on}/I_{off} \sim 10^7$ is observed, and the subthreshold slope (SS) is estimated SS ≈ 1150 mV/dec from the forward sweep at V_{DS} = 0.1 V. We note the SS is relatively high but can be reduced by decreasing the equivalent oxide thickness of the gate dielectric below the 50 nm SiO_2 used here. Reducing interface charge trap density at the MoS_2/dielectric interface[58] by passivating the dielectric[59] or by using a molecular crystal seeding layer[60] can also greatly improve the SS when employing cleaner, dedicated fabrication outside general-purpose academic facilities.

Figure 3b shows the measured I_D versus V_{DS} output curves at back-gate voltages from V_{GS} = 5 to 20 V for the same L_{ch} = 100 nm device. The maximum drive current achieved was $I_{D,max} \sim 140\ \mu A/\mu m$ at V_{DS} = 1 V and V_{GS} = 20 V, which is the highest reported for monolayer MoS_2 grown below 600 °C. Current saturation is not observed because the threshold voltage V_T is sufficiently small to keep this device in the linear operating region throughout. Relatively low hysteresis is again observed from the forward and backward voltage sweeps, indicating minimal charge trapping. The measured I_D versus V_{GS} transfer curves at V_{DS} = 0.1 V for channel lengths from L_{ch} = 100 to 700 nm are shown in Figure 3c. The threshold voltage V_T ranges from 2.4 to 5.8 V using the linear extrapolation method.[16] The measured I_D versus V_{DS} output curves at V_{GS} = 20 V for channel lengths from L_{ch} = 100 to 700 nm are shown in Figure 3d. I_D decreases for increasing channel lengths, as expected, due to larger channel resistance contribution for a constant V_{DS} and a constant contact resistance (R_C).

We next turn to estimating R_C first and then the electron mobility from TLM structures. In addition to a better estimation of R_C, the MoS_2 channel sheet resistance (R_{sh}) can also be accurately extracted from the slope of the linear

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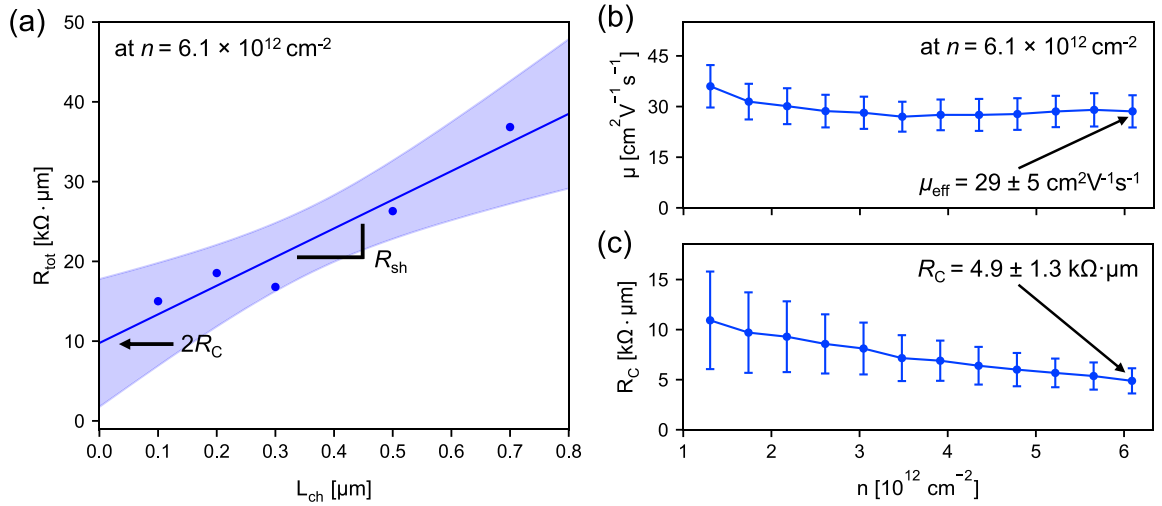

Figure 4. Sheet resistance and mobility. (a) Linear TLM fit of the total measured resistance (R_{tot}, normalized by channel width) as a function of the channel length (L_{ch}) at a carrier concentration n = 6.1 × 10^{12} cm^{-2}, corresponding to the same gate overdrive, $V_{OV} = V_{GS} - V_T$ = 14 V. The y-intercept corresponds to twice the contact resistance ($2R_C$), while the slope of the line is the sheet resistance (R_{sh}). The shaded region marks the 95% confidence bound of the line fit. (b) Effective mobility (μ_{eff}) vs n as obtained from the sheet resistance. Here, μ_{eff} = 29 ± 5 cm^2 V^{-1} s^{-1} at n = 6.1 × 10^{12} cm^{-2}, which is comparable to previous reports of monolayer MoS_2 grown at higher temperatures (see Figure 5). (c) Contact resistance (R_C, normalized by width) as a function of the carrier concentration, n. The contact resistance was down to R_C = 4.9 ± 1.3 kΩ·μm at n = 6.1 × 10^{12} cm^{-2}. All measurements were taken at V_{DS} = 0.1 V and room temperature in a vacuum probe station.

TLM extrapolation. The sheet resistance is then used to estimate the effective mobility, $\mu_{eff} = (qnR_{sh})^{-1}$, where q is the elementary charge and n is the electron density per unit area. Here, $n = C_{ox}(V_{GS} - V_T - V_{DS}/2)/q$ as all our transistors remain in the linear regime, where C_{ox} is the gate dielectric capacitance per unit area (~70 nF/cm^2 for our 50 nm SiO_2). We note V_T must be individually assessed for each channel in the TLM to account for any device-to-device variation.

Figure 4a shows the linear TLM fit of the total measured resistance ($R_{tot} = L_{ch}R_{sh} + 2R_C$, normalized by width) versus channel length (L_{ch}) extracted from Figure 3d at a carrier concentration n = 6.1 × 10^{12} cm^{-2} (at the same gate overdrive, $V_{OV} = V_{GS} - V_T$ = 14 V, not the same gate voltage V_{GS}). V_T is extracted for each channel length in Figure 3c by the linear extrapolation method.[57,61] The y-intercept of the linear fit in Figure 4a corresponds to the total contact resistance, $2R_C$. We note that it is important to perform such TLM fits using a wide range of channel lengths (from short, dominated by $2R_C$, to long, dominated by $L_{ch}R_{sh}$) in order to minimize the R_C extrapolation error. The remaining uncertainty of the linear TLM fit represents the intrinsic device-to-device variation. Figure 4b shows the effective mobility (μ_{eff}) as a function of carrier concentration n, obtained from the TLM plot slope, which is the sheet resistance (R_{sh}). At n = 6.1 × 10^{12} cm^{-2}, the effective electron mobility is μ_{eff} = 29 ± 5 cm^2 V^{-1} s^{-1}, which is comparable to mobilities reported at higher growth temperatures.[13,16,28−31,33,34] Figure 4c shows the contact resistance (R_C, normalized by width) also as a function of the carrier concentration n. The contact resistance was R_C = 4.9 ± 1.3 kΩ·μm at n = 6.1 × 10^{12} cm^{-2} with the error bound corresponding to the 95% confidence interval of the line fits.

In Figure 5 we compare the room-temperature electron mobility data of our films grown at 560 °C with previous reports for other CVD-grown (and MOCVD-grown[36−41]) 1L MoS_2 reported in the literature,[13,16,18,20,28−30,32,34,62−67] as a function of the growth temperature. We note that some reports are given as effective mobility[13,16,28−30] (μ_{eff} from TLM, denoted by squares); others are only available as field-effect

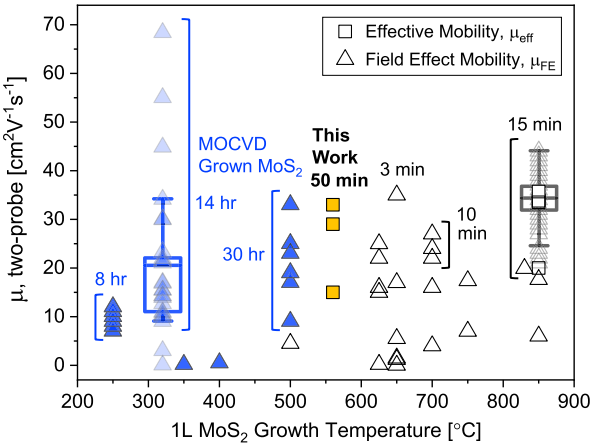

Figure 5. Monolayer MoS_2 electron mobility vs growth temperature. Reported effective mobilities (μ_{eff} from TLM) are squares and two-probe field-effect mobilities (μ_{FE}) are triangles. μ_{eff} from this report are marked in yellow. MOCVD data[36−41] are μ_{FE} marked in blue, and solid-source CVD data from the literature[13,16,18,20,28−30,32,34,62−67] are hollow symbols. Growth times (at maximum process temperature) are also labeled, indicating significantly longer growths reported for MOCVD to attain full coverage 1L MoS_2. The CVD films in this work were grown at 560 °C for 50 min, while MOCVD films were grown at or below 500 °C for 8 to 30 h,[36−41] as labeled. The μ_{eff} from sheet resistance (TLM) measurements tend to be more reliable, while μ_{FE} could be under- or overestimated depending on the V_{GS}-dependence of gated contacts.[68,73,74] All mobility data are reported at room temperature. During review, we became aware of recent MOCVD films grown at 320 °C for over 14 h;[37,38] a summary of μ_{FE} data for these films (lighter blue triangles) is shown as the box-and-whisker plot at 320 °C (average μ_{FE} of 20.4 cm^2 V^{-1} s^{-1} in the blue box).

mobility[18,20,32,34,36,62−67] (μ_{FE}, denoted by triangles). The effective mobility values from this work (grown at 560 °C for 50 min) are marked in yellow. The field-effect mobility values reported from MOCVD growths (at or below 500 °C for 8 to 30 h) are marked in blue.[36−41] For this simple comparison, we

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benchmark two-probe mobility measurements, although more complex four-probe measurements with a threshold voltage correction can yield more accurate mobility values[68] if current shunt paths through the (invasive) inner voltage probes are avoided.[7] In general, we have found no correlation between carrier mobility and growth temperature, only between growth temperature and MoS_2 crystallite size or substrate adhesion. Growth times (at maximum process temperature) are also labeled, indicating significantly longer growths reported for MOCVD to attain full coverage 1L MoS_2.

First, comparing the effective 1L MoS_2 mobilities (μ_{eff}, squares), we observe that our values (29 and 33 $cm^2\ V^{-1}\ s^{-1}$ from 560 °C growths at a reduced 490 Torr pressure) are similar to the μ_{eff} from MoS_2 grown at higher temperatures, up to 850 °C.[13,16,28−30] (Recent simulations have shown that mobilities in this range are limited by point defects, most likely, charge impurities and sulfur vacancies.[69,70]) Field-effect mobility (μ_{FE}) data reported for 1L MoS_2 grown at 850 °C (lighter hollow triangles) are also included as a box-and-whisker plot (average μ_{FE} of 34.2 $cm^2\ V^{-1}\ s^{-1}$ outlined in the black box),[16] in good agreement with the 850 °C effective mobility. For CVD-grown 1L MoS_2 using solid-source precursors, our values are the highest reported mobilities to date with a thermal budget below 2 h at 600 °C. One notable difference is that our past 850 °C growths have yielded up to ∼10% bilayer regions,[16] while such bilayer regions are undiscernible on the 560 °C growths presented here (Figure 1). In addition, we have also found the MoS_2 grown at 560 °C to be more weakly adhered to the SiO_2 substrate compared to our previous studies at higher growth temperatures,[13,16,28−30] which necessitated careful electron-beam lithography without exposing the MoS_2 samples to water to avoid delamination during processing.[71,72] We note that adhesion challenges, in addition to the growth residue observed on the 1L MoS_2 grains and along the grain edges, could have also led to some of our observed device-to-device variation.

When comparing effective mobility values with field-effect mobilities (μ_{FE}, triangles) reported across the literature, most μ_{FE} reported are lower. This is mainly due to the effects of the contact resistance, although material quality, nonideal contact selection, and device fabrication (in academic facilities) could also cause the large μ_{FE} variation observed, with no clear trends between studies and across growth temperatures. It is also possible that μ_{FE} is overestimated in some studies depending on the gate-voltage-dependence of the contacts. In other words, a sharp turn-on of back-gated contacts can lead to an overestimated peak transconductance g_m and μ_{FE}.[68,73,74] Due to these effects of gated contacts, effective mobility (μ_{eff}) from sheet resistance (TLM) measurements (particularly when reported as a function of the carrier density n) tend to be more reliable and are preferable, rather than μ_{FE}, as the main figure of merit for MoS_2.

CONCLUSIONS

We have demonstrated direct CVD solid source precursor growth of monolayer (1L) MoS_2 at 560 °C in 50 min, with electrical and optical properties very similar to those of CVD MoS_2 grown at higher temperatures. Our films are within the 450-to-600 °C, 2 h thermal budget window required for BEOL compatibility with modern silicon integrated circuit processing. These new 1L MoS_2 films growths were enabled by carefully matching an optimized sulfur flux to sufficient volatile MoO_{3-x} reduced in the presence of the carbon-based PTAS seed layer. Electrical measurements revealed a maximum drive current $I_{D,max} \sim 140\ \mu A/\mu m$ at $V_{DS} = 1$ V, which is the highest reported for 1L MoS_2 grown below 600 °C using solid-source precursors. The effective electron mobility was extracted with TLM test structures as $\mu_{eff} = 29 \pm 5\ cm^2\ V^{-1}\ s^{-1}$ at a carrier concentration of $6.1 \times 10^{12}\ cm^{-2}$, which is comparable to mobilities reported from films grown at higher temperatures. The results of this work provide a path toward the realization of high-quality, thermal-budget-compatible TMDs for heterogeneous integration with silicon manufacturing. These could enable 3D integration of such 2D materials for advanced functionalities in memory or power-gating circuits (with low-leakage BEOL transistors) or high-density logic in the third dimension.

METHODS

560 °C 1L MoS_2 CVD Growth. PTAS dissolved in water was deposited as droplets around the perimeter of 1.5 × 2 cm chips of thermally grown 50 nm SiO_2 on p^+ silicon that were initially rinsed with deionized water.[13] The PTAS droplets dried into "coffee rings" around the perimeter of the substrate before the seeded SiO_2/Si chips were placed face-down on top of an alumina (Al_2O_3) crucible containing ∼2 mg of MoO_3 powder (Alfa Aesar, Puratronic 99.9995% purity) spread into a ∼1 cm diameter circle. ∼100 mg of excess solid sulfur source (Alfa Aesar, Puratronic 99.999% purity) melted in a quartz boat was placed ∼26 cm away from the center near the incoming Ar gas flow inlet, all enclosed within a 55 mm inner diameter quartz tube. Before each growth, the system was flushed for 5 min using 1500 sccm Ar gas under vacuum before setting the ambient condition to 490 Torr at 22 sccm Ar flow rate, adjusting the throttle valve. For the growth temperature cycle, the tube furnace was first ramped from room temperature to 450 °C in 10 min and then subsequently ramped to 560 °C in 5 min. The temperature was held at 560 °C for 50 min before rapidly cooling down to room temperature by opening the furnace hatch. The partially reduced MoO_3 source must be cleaned out and replenished after each growth cycle, while the excess solid sulfur source can be reused in subsequent growths.

MoS_2 Device Fabrication. Contact probe pads and coarse contacts were defined by e-beam lithography using a bilayer resist stack of 250 nm methyl methacrylate (MMA)/50 nm poly (methyl methacrylate) (PMMA). This promotes resist undercutting for easier contact metal liftoff which helps maintain MoS_2 adhesion to the growth substrate. This was followed by e-beam evaporation of 20 nm SiO_2/2 nm Ti/70 nm Au, all layers deposited at 0.5 Å/s at a base-pressure of 10^{-7} Torr. The 20 nm SiO_2 layer helps mitigate pad-to-gate leakage through the back-gate dielectric. This was followed by an overnight liftoff in acetone at room temperature. Fine contacts were patterned using e-beam lithography with a 60 nm PMMA 495k/215 nm PMMA 950k bilayer resist stack which provides fine resolution along with sufficient undercutting for effective liftoff. 70 nm Au was then deposited by e-beam evaporation at a deposition rate of 0.5 Å/s at a base pressure below 10^{-7} Torr without any adhesion layer to achieve a clean contact interface. The liftoff was carried out in Remover PG solvent for 30 min at 80 °C. MoS_2 was patterned into uniform rectangular channels of 2 μm width by photolithography followed by a gentle O_2 plasma etch. The O_2 plasma etch was carried out at a power of 10 W in a chamber set to 20 mTorr pressure and 20 sccm O_2 flow rate for 60 s.

Optical, Electrical, and AFM Characterizations. Raman and PL data were take in air, at room temperature, using a HORIBA Labram with a 532 nm excitation laser. All electrical measurements were at room temperature, in the dark and under vacuum ($<10^{-5}$ Torr) after an in situ vacuum anneal at 250 °C for 2 h, in a Janis ST-100 probe station. SEM was conducted using a Thermo Fisher Scientific Apreo S SEM equipped with a NiCol electron column operated in the immersion mode. AFM was conducted using a Bruker Dimension Icon AFM system operated in the tapping mode.

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Author Contributions

A.T. and A.K. contributed equally. A.T., A.K., and E.P. conceived the experiments and wrote the manuscript with input from all authors. A.T. grew MoS_2 and performed the Raman and PL characterizations. A.K. and M.J. performed the SEM and AFM characterizations, respectively. A.K., M.J., and A.T. fabricated the devices. A.K. and A.T. performed the electrical measurements and data analysis.

Notes

The authors declare no competing financial interest.

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