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Low Variability in Synthetic Monolayer MoS_2 Devices

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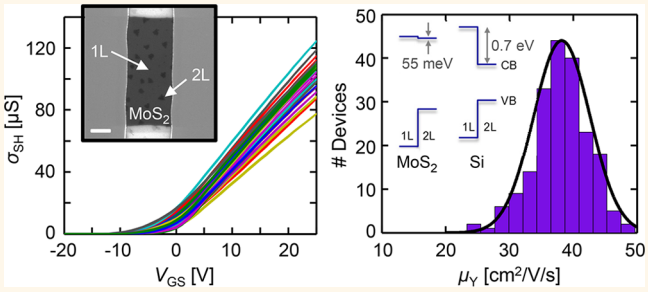
Supporting Information

ABSTRACT: Despite much interest in applications of two-dimensional (2D) fabrics such as MoS_2, to date most studies have focused on single or few devices. Here we examine the variability of hundreds of transistors from monolayer MoS_2 synthesized by chemical vapor deposition. Ultraclean fabrication yields low surface roughness of ~3 Å and surprisingly low variability of key device parameters, considering the atomically thin nature of the material. Threshold voltage variation and very low hysteresis suggest variations in charge density and traps as low as $\sim 10^{11}$ cm^{-2}. Three extraction methods (field-effect, Y-function, and effective mobility) independently reveal mobility from 30 to 45 cm^2/V/s (10th to 90th percentile; highest value ~48 cm^2/V/s) across areas >1 cm^2. Electrical properties are remarkably immune to the presence of bilayer regions, which cause only small conduction band offsets (~55 meV) measured by scanning Kelvin probe microscopy, an order of magnitude lower than energy variations in Si films of comparable thickness. Data are also used as inputs to Monte Carlo circuit simulations to understand the effects of material variability on circuit variation. These advances address key missing steps required to scale 2D semiconductors into functional systems.



KEYWORDS: *MoS_2, chemical vapor deposition, variability, mobility, threshold voltage, band offsets*

As the study of two-dimensional (2D) materials continues into its second decade, functionality beyond individual devices is gaining importance and being explored in the form of simple circuits implemented in graphene[1−3] and transition-metal dichalcogenides (TMDs).[4,5] Further implementation of realistic systems based on 2D semiconductor TMDs must rely on large-area films grown, *e.g.*, by chemical vapor deposition (CVD). Recent studies have shown steady and increasing improvement in metrics such as mobility and contact resistance for CVD-grown MoS_2,[6,7] facilitated in part by recent progress in transfer[8−10] and CVD processes.[11−15] However, CVD-grown monolayer (1L) semiconductors present distinctive sources of variability, such as crystal orientation, grain boundaries, and small islands of bilayer (2L) regions. Only a few TMD studies have looked beyond individual devices,[16,17] and a thorough investigation into intrinsic material variability, its physical origins, and how it will affect system performance is presently lacking.

Herein we explore this variability for important metrics such as threshold voltage (V_T), charge trap density (n_t), current max/min ratio, mobility, and hysteresis (H) of hundreds of transistors fabricated from >1 cm^2 areas of CVD-grown monolayer MoS_2 films. These 2D fabrics achieve metrics (*e.g.*, low hysteresis, high mobility) on par with or better than other CVD-grown films reported to date. In addition, we find that the electrical effects of TMD thickness variation (*e.g.*, 1L to 2L) are an order of magnitude less severe than would be expected for silicon films of comparable thickness. We also use our data as inputs for Monte Carlo simulations of standard logic cells and analyze the effect that intrinsic material variability has on key system properties, including energy consumption and delay. Such insight into the variability of 2D semiconductors is crucial for future applications, and for comparison to technologies such as ultrathin body silicon-on-insulator (UTB SOI) or oxide semiconductors which could potentially be replaced or complemented by TMDs.[18−21]

RESULTS AND DISCUSSION

As shown in Figure 1, we employ large-area MoS_2 films grown by CVD directly on t_{ox} = 30 nm SiO_2 on cm-scale Si substrates, which also serve as back gates. The CVD growth details are reported in the Methods section and ref 15. The back gate oxides have measured $C_{ox} \approx 116$ nF/cm^2 and negligible leakage

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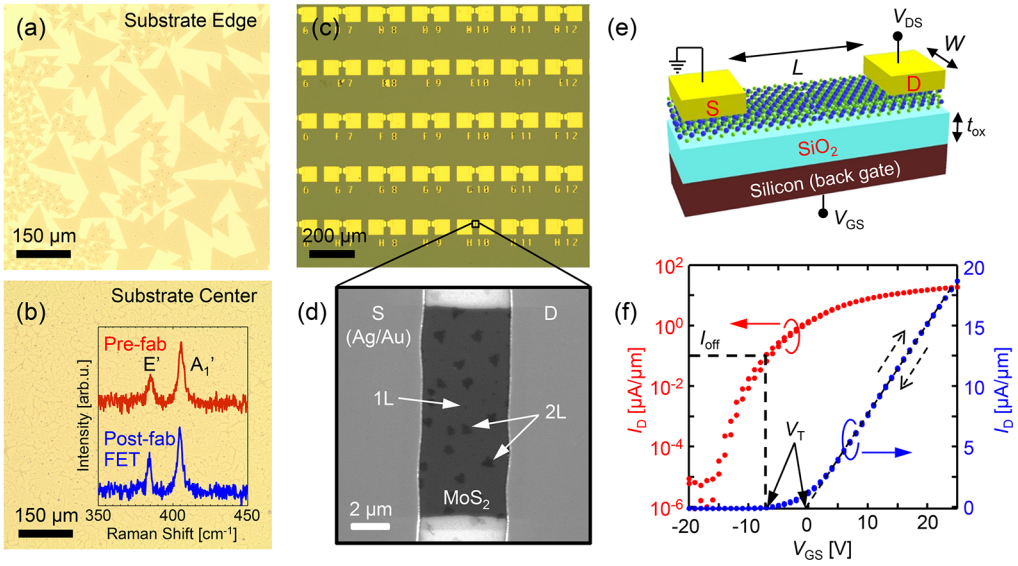

Figure 1. (a) Optical image near the edge of the growth substrate. Darker, triangular MoS_2 grains can be seen (typically >100 μm across) and lighter areas are SiO_2. (b) Image of continuous MoS_2 fabric near the center of growth substrate. Inset: Raman spectra of the MoS_2 and a fabricated FET channel, showing no change. (c) Optical image of a portion of the chip with finished devices. (d) SEM image of a MoS_2 FET with Ag/Au contacts, from which L and W are measured. (e) Schematic of FETs, labeling dimensions, and biasing scheme. (f) Forward and backward I_D–V_{GS} data at V_{DS} = 1.0 V for the device in Figure 1d, plotted in both linear (blue) and logarithmic (red) scale, revealing very low hysteresis. The dashed line on the linear data shows the extrapolation for the linear V_T extraction. Dashed lines on the log data correspond to I_{off} = 100 nA/μm. This illustrates how different V_T can be obtained from linear extrapolation and constant-current methods.

up to 25 V (see Supporting Information Figure S1). The cm^2 MoS_2 films are continuous large-grain 1L with a small fraction being bilayer (2L) regions, as shown in Figure 1a,b. Optical lithography is used to fabricate hundreds of field-effect transistors (FETs) of varying length and width (L and W) on a single chip, as seen in Figure 1c, and fabrication details are provided in the Methods section and Supporting Information section B. A top-view scanning electron microscope (SEM) image and a cartoon of the device geometry are shown in Figure 1d,e, respectively. Small 2L regions ($\leq$0.5 μm^2) are visible in the channel, which is itself a single 1L crystal, as the grain size of these films is ~100 μm.

Electrical Measurements. Direct current (DC) electrical characteristics of 200 devices were measured to give statistical data for threshold voltage V_T, density of charge traps n_t, hysteresis H, I_{max}/I_{min} current ratio, and three definitions of mobility: field-effect μ_{FE}, Y-function μ_Y, and effective mobility μ_{eff} (see Methods). Such data consist primarily of forward–backward I_D–V_{GS} sweeps (at V_{DS} = 0.1 and 1.0 V), as shown in Figure 1f. V_T was extracted using four methods from the I_D–V_{GS} sweeps:[22,23] linear extrapolation, constant-current (CC), $(I_D)^{1/2}$, and Y-function methods. Only the well-known linear extrapolation method is analyzed in depth here, as its variation directly corresponds to variation in charge density. An upper bound of $n_t = \Delta V_T C_{ox}/q$ is estimated conservatively by finding the difference ΔV_T between forward and backward sweeps,[24] where q is the elementary charge. The ratio of maximum to minimum current is I_{max}/I_{min}, employed here because the "on/off ratio" is not well-defined without given voltage rails in a circuit (see Supporting Information Figure S5). The μ_{FE} is proportional to the maximum transconductance ($g_m = \partial I_D/\partial V_{GS}$), as $\mu_{FE} = g_m L(WC_{ox}V_{DS})^{-1}$. H is the maximum measured difference in constant-current voltage from the forward and backward sweeps across the entire linear portion of the curve (note that it is very small for our devices). We also quantify W and L, the fabricated device widths and lengths as measured by SEM (summarized in Supporting Information Figure S7).

For all 200 devices, we calculate the mean and standard deviation of these device variability parameters, exemplified in Figure 2a–f with histograms and Gaussian or log-normal fits to the distributions for V_{DS} = 1.0 V. (Similar data taken for V_{DS} = 0.1 V are given in Supporting Information section D.) Figure 2a shows the extracted V_T as defined by the CC method (with I_{off} = 100 nA/μm, based on high-performance device specifications of the International Technology Roadmap for Semiconductors)[25] and by linear extrapolation for the forward sweep. [V_T extraction from $(I_D)^{1/2}$ and Y-function methods are shown in Supporting Information Figure S2.] We find the V_T distributions for all four definitions to be Gaussian, and the standard deviation for the linear extrapolation s_{V_T} = 1.10 V corresponds to a variation in charge carrier density by $s_n = s_{V_T}C_{ox}/q = 8 \times 10^{11}$ cm^{-2}.

To put these values in context, we note that they correspond to our monolayer (6.15 Å thin) MoS_2 with the back gate oxide thickness used here, t_{ox} = 30 nm. These charge variations are very small and already lower than those predicted for 2 nm thick UTB SOI silicon FETs,[26] which are expected to have $s_n \approx 1.5 \times 10^{12}$ cm^{-2} due to body thickness variation alone, for the corresponding s_{V_T} and equivalent oxide thickness (EOT). In other words, if the EOT of our devices were scaled to 0.9 nm, our MoS_2 devices would have s_{V_T} = 33 mV across >1 cm^2 areas, suggesting that such CVD-grown 2D semiconductors today already have lower variability issues than silicon films only a few nm thick. For 2D semiconductors, these metrics could be improved with additional growth and process improvements, but for ultrathin silicon films, these are fundamentally limited by thickness variation and random dopant fluctuations. Thus, by its 2D nature, MoS_2 circumvents many issues faced by a 3D semiconductor (like Si) in UTB SOI, for which manufacturable

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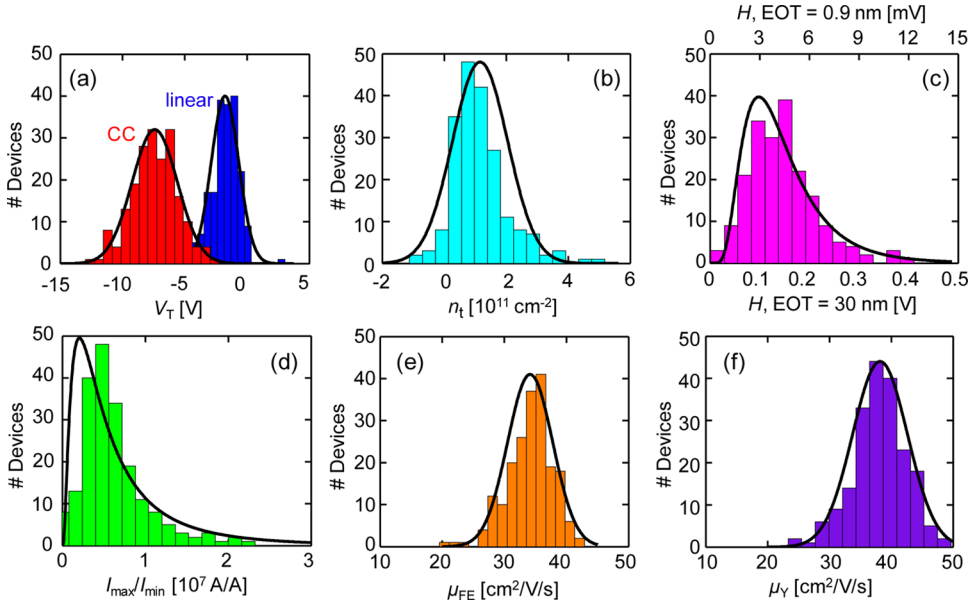

Figure 2. Histograms and distribution fits of statistical data. (a) V_T for both the linear extrapolation (blue) and constant-current (I_{off} = 100 nA/μm, red) methods. (b) n_t as estimated from ΔV_T. (c) Hysteresis in forward−backward I_D−V_{GS} sweeps, which we observe to follow a log-normal distribution. Top horizontal axis shows the very small hysteresis expected if the EOT is scaled to 0.9 nm. (d) I_{max}/I_{min} is also log-normal, since subthreshold current is exponentially dependent on V_T. (e and f) Histogram of mobility values as extracted from (e) the field-effect and (f) the Y-function approach. Note that $\mu_Y > \mu_{FE}$ in all cases due to the differences in extractions methods.

solutions are not currently known beyond the 5 nm technology node.

ΔV_T for our devices is also Gaussian, with a mean value of $\langle \Delta V_T \rangle$ = 0.16 V, corresponding to $n_t = 1.1 \times 10^{11}$ cm^{-2}, as summarized in Figure 2b. This value implies that lower densities of charge traps are present in high-quality CVD-grown MoS_2 (and at the SiO_2 interface) than previously suggested for some exfoliated samples.[27,28] A further indication of charge trapping is the measured constant-current hysteresis H,[29] which we find to have a mean and standard deviation $\langle H \rangle$ = 0.14 V and s_H = 0.07 V (Figure 2c), indicating that our devices are largely independent of their own bias history for electric fields up to 0.25 V/μm laterally and 1 V/nm vertically. For the decile of devices with the lowest hysteresis, these 20 all demonstrated $H \leq 50$ mV. While these values are obtained for t_{ox} = 30 nm, scaling to an EOT = 0.9 nm would give a very small average $\langle H \rangle \approx 4.2$ mV, as shown along the top horizontal axis of Figure 2c. This is much smaller than the supply voltages of modern circuits, and thus large-scale implementation of CVD-grown MoS_2 is already not hindered by intrinsic variability today, provided the EOT is scaled accordingly.

Figure 2d reveals that the measured I_{max}/I_{min} ratio follows a log-normal distribution. This is unsurprising given that s_{V_T} is normally distributed and the subthreshold current $I_{sub} \propto \exp(V_{GS} - V_T)$.[30] For our devices, the median measured $I_{max}/I_{min} = 5.3 \times 10^6$ A/A, keeping in mind that actual current ratios could be higher, as I_{min} can be limited by the measurement noise floor (~ pA here, as seen in Figure 1f). Additional visualizations of these data and the rest that follow are available in the Supporting Information sections C and D, in the form of cumulative distribution functions and box-and-whisker plots.

In order to decouple the measured electrical variation from geometric variation, all devices were measured by SEM to obtain precise values for L and W. Figure 2e shows the field-effect mobility distribution, with mean $\langle \mu_{FE} \rangle$ = 34.2 cm^2/V/s and standard deviation $s_{\mu_{FE}}$ = 3.6 cm^2/V/s, which yields a coefficient of variation $CV_\mu = s_\mu/\langle \mu_{FE} \rangle$ = 0.10. W and L, on the other hand (Supporting Information Figure S7), were measured to have CV_W = 0.01 and CV_L = 0.05. This implies that, given nominal values of L and W, the CV for *nominal* μ_{FE} based on what the dimensions of the devices *should* be (rather than what they actually *are*) is[31] $(CV_L^2 + CV_W^2 + CV_\mu^2)^{1/2}$ = 0.12. In other words, variations in lithographic features here are sufficiently small that the device behavior has a variation only 2% larger when assuming L and W are their average values from lithography. Indeed, this is exactly what we observe: When assuming that L and W are their average values and repeating the analysis, $\langle \mu_{FE} \rangle$ remains 34.2 cm^2/V/s while the standard deviation $s_{\mu_{FE}}$ slightly increases to 4.1 cm^2/V/s, resulting in CV = 0.12 (see Supporting Information Figure S8).

To further analyze mobility, we employ the Y-function method, (see ref 23 and Supporting Information section E), whereby we calculate μ_Y = 38.2 ± 8.8 cm^2/V/s and R_{CY} = 3.0 ± 1.4 k$\Omega \cdot \mu$m (see Figure 2f and Supporting Information Figure S9), where the uncertainties here are indicative of two standard deviations (95% inclusive). We note that this estimation of contact resistance is an upper bound and that the true R_C could be lower. The 10th to 90th percentile of mobilities extracted by the field-effect and Y-function methods ranges from 30 to 45 cm^2/V/s (highest value ~48 cm^2/V/s from the Y-function approach). Additionally, we note that the mobility extracted from the Y-function approach is slightly higher than the other methods because the Y-function typically gives a higher V_T than the linear extrapolation method.[32]

Linear and log-scale data for the sheet conductance [$\sigma_{SH} = I_D L/(V_{DS} W)$] of an example 30 of our devices are plotted in Figure 3a and its inset, respectively, at V_{DS} = 0.1 V. These types of measurements across the entire data set were used for pseudo-transfer length method (pTLM) analysis. Unlike the linear TLM, where resistances of several channel lengths are measured along the same material strip with shared contacts,[33] for the pTLM we measure resistances (R_{TOT}) of all our devices

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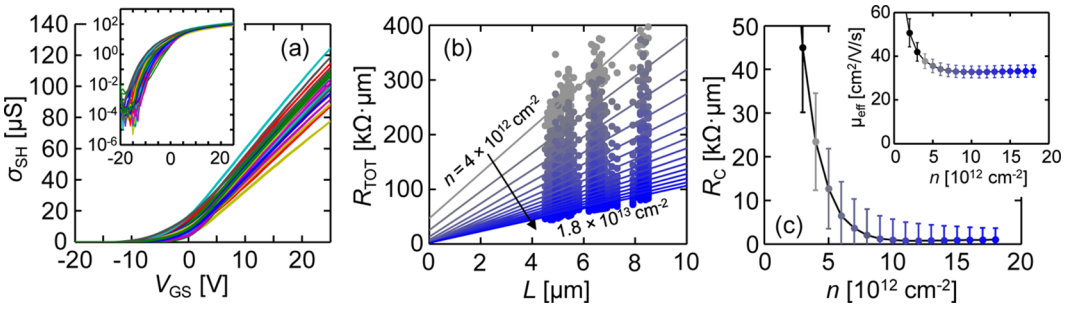

Figure 3. (a) Sheet conductance σ_{SH} *vs* V_{GS} for a representative sample of 30 devices. The inset shows the same data displayed in log scale. The V_T variation seen here corresponds to a subset of that recorded in Figure 2a. The EOT here is 30 nm, however if this were scaled to 0.9 nm, these MoS_2 devices would have s_{V_T} = 33 mV across >1 cm^2 areas (see text). (b) Pseudo-TLM (pTLM) analysis showing measured R_{TOT} vs L (symbols) for the 10th through 90th percentile of devices at n = 4 to 18 × 10^{12} cm^{-2}, with linear regression fits. The color gradient marks the increasing carrier density. The slope of the linear fits corresponds to the sheet resistance $R_{SH} = (qn\mu_{eff})^{-1}$, and the abscissa intercept is $2R_C$. (c) R_C *vs* n as extracted from the pTLM, with error bars reflecting 95% confidence intervals and a minimum of 730 Ω·μm at $n \approx 1.3 \times 10^{13}$ cm^{-2}. Inset: Effective mobility μ_{eff} *vs* n for the same fitting, reaching ~34 cm^2/V/s for all $n \geq 4 \times 10^{12}$ cm^{-2}.

with various L and W distributed across the chip, constructing the scatter plot in Figure 3b. We fit the linear regression lines to the 10th through 90th percentiles of devices, noting that R_{TOT} distributions are Gaussian with respect to L and W. The vertical intercept of the pTLM line fits is twice the contact resistance, and the slope is the sheet resistance, which can be used to estimate the effective mobility. In Figure 3c this analysis yields values for μ_{eff} = 33.8 ± 2.8 cm^2/V/s and R_C = 1.0 ± 2.6 kΩ·μm at n = 1.8 × 10^{13} cm^{-2}, where the uncertainties reflect 95% confidence intervals in the fitting. We note that despite the uncertainty of contact resistance in the pTLM method, the range of R_C reported in this work for all extraction methods is among the best reported today for monolayer, undoped MoS_2. We attribute these results to the cleanliness of our process conditions and the use of Ag/Au contacts deposited in ultrahigh vacuum (see Supporting Information Section B).

It is important to emphasize that all figures of merit discussed here are for monolayer, CVD-grown MoS_2, a sub-1 nm thin semiconductor. In contrast, silicon has an effective mobility of ~2 cm^2/V/s for comparable thickness and carrier densities[34] due to strong surface roughness scattering and atomic-scale thickness fluctuations. However, it is evident even from micron-scale devices that improvements in contact engineering are currently the greatest issue facing the scaling of TMD systems from a device perspective. The contact resistance achieved here on a large scale is of the order 1.0 kΩ·μm for $n \geq 10^{13}$ cm^{-2}, among the best reported for a monolayer semiconductor without deliberate doping. This must be further lowered by up to an order of magnitude, as devices <100 nm would be ~50% contact dominated with similar contacts.[33]

Surface Imaging and Analysis. To gain physical insight into why our MoS_2 devices show relatively low variation given the atomically thin nature of this material, we perform measurements including atomic force microscopy (AFM), scanning Kelvin probe microscopy (SKPM), and SEM analysis of grain boundaries on the fabricated devices. The surface roughness of our MoS_2 FETs is quantified *via* AFM including the 2L regions as shown in Figure 4a, and the root-mean-square (RMS) value is only 3 Å (Figure 4b) *after fabrication*, which is near the limit of AFM capabilities and comparable to similar measurements on freshly exfoliated MoS_2 on SiO_2.[35] We attribute this low roughness as well as the negligible hysteresis and low variability of our devices in part to our growth and processing methods (Supporting Information section B), which yield devices remarkably free of cracks, wrinkles, or photoresist residue. The small tail at the upper end of the curve in Figure 4b is due to the 2L regions, and the distribution does not change if sampling over the entire FET channel. Figure 4c shows the 1L−2L junction step height measured by AFM is $\Delta z_{1L-2L} \approx 6$ Å, in agreement with the two Gaussian fits in Figure 4b as well as the 6.15 Å MoS_2 layer separation observed by neutron diffraction studies on bulk samples.[36]

SKPM imaging in Figure 4d,e reveals the contact potential difference (CPD) at 1L−2L boundaries is only ~55 meV, confirming recent studies which have shown that 1L−2L MoS_2 conduction band (CB) offsets are relatively small, $\Delta E_{CB} \sim 2k_BT$ at room temperature.[37,38] The surface potential "jumps" at the 2L edges are due to the higher reactivity of the edges,[39,40] ostensibly from adsorbates accumulated during long SKPM measurements in air. To compare these findings with variability in ultrathin silicon, we turn to Figure 4f. This illustrates that ΔE_{CB} in MoS_2 is over an order of magnitude smaller than CB offsets calculated for comparable thickness variation (1L *vs* 2L) in Si, which are ~0.7 eV depending on crystal orientation.[41,42] Thus, in addition to robustness against short-channel effects in ultrathin body transistors, 1L MoS_2 films also offer natural robustness to fluctuations in V_T and on-state electron density caused by thickness irregularities. For n-type applications the CB variation is nearly negligible at room temperature, since the majority of the potential discontinuity occurs in the valence band of MoS_2.[37] Other monolayer semiconductors will need to be similarly evaluated for variation (or lack thereof) in p-type applications.

SEM images of our fabricated FETs (such as Figure 1d) also reveal that, out of 200 channels with ~10 μm^2 area, 116 are single-crystal, 75 have a single grain boundary (GB), and 9 have two GBs. However, the presence of GBs does not appear to affect device performance to a significant degree, consistent with previous results.[43] Similar to 1L−2L junctions, Huang *et al.* (ref 37) found that CB offsets at GBs are also small and most energy discontinuities occur in the valence band. Note that all our measured device variability *includes* random distributions of 2L islands and ~40% of our devices have at least one GB. We do not observe bi- or trimodal distributions in our data and thus conclude (supported by our and others' surface analysis) that the electrical variability introduced by small 2L regions and GBs is minimal for n-type monolayer MoS_2 nanofabrics operating at room temperature.

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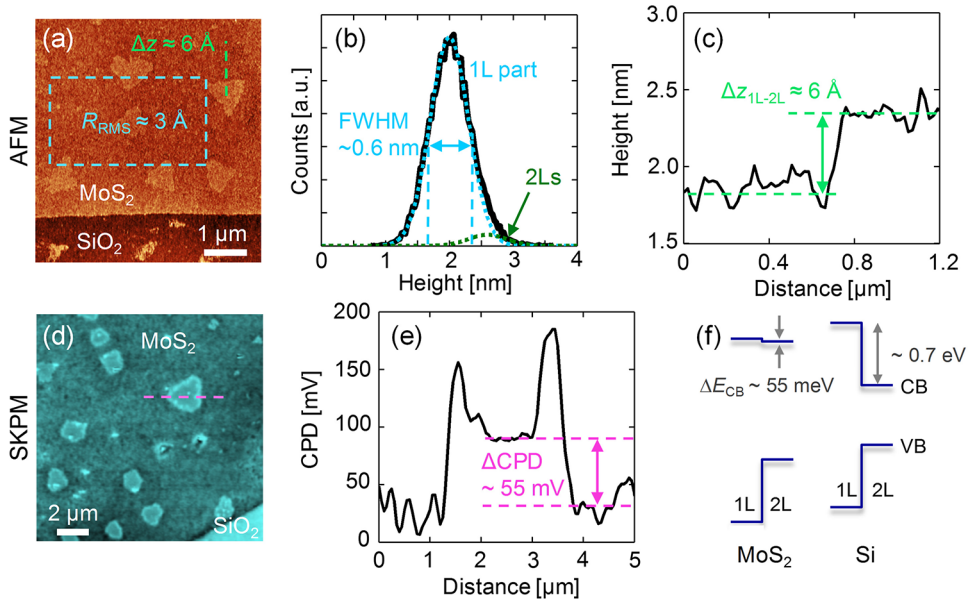

Figure 4. (a) AFM image of the edge of a fabricated channel, showing small 2L regions. (b) Probability distribution of height measurements for the blue boxed region in (a). The full-width at half-maximum (fwhm) is twice the measured RMS roughness, ~3 Å, including the 2L islands. (c) The height profile of the 1L−2L step shows $\Delta z_{1L-2L} \approx 6$ Å. (d) SKPM image of a fabricated channel. (e) Contact potential difference (CPD) across a 1L−2L junction, revealing ~55 mV offset. (f) Schematic energy band diagrams at a 1L−2L MoS_2 junction and for Si films with comparable thickness variation. The conduction band (CB) variation of MoS_2 is over an order of magnitude smaller, making this material much more immune to thickness variation than ultrathin "bulk" semiconductors such as Si.

Circuit Modeling of Variation. We now use our measured device-to-device variation to predict its possible impact on circuit performance and variability. To this end, we perform Monte Carlo simulations of standard cells for transistor technologies with channel length L = 16−500 nm. For simplicity, we restrict our analysis to two-input NAND and NOR gates with channel widths of 1 μm and loaded with 1 pF output capacitance. (Schematics are shown in Supporting Information Figure S13.) This methodology, however, can be easily extended to any standard cell made from 2D transistors. To perform this analysis, we rely on our physics-based compact model developed for 2D semiconductor FETs[44,45] which includes fringing capacitances, contact resistance, saturation velocity, device self-heating, and proper electrostatics. The model is fit to our experimental data, but otherwise assumes R_C and EOT based on Technology Roadmap specifications,[25] with I_{off} = 100 nA/μm for high-performance applications. Specifically, R_C varies from 188 to 200 Ω·μm, and EOT varies from 0.8 to 5 nm (see Supporting Information sections F and G). To achieve complementary logic, we mimic p-type transistors using the device parameter distributions of the n-type transistor. We do, however, consider other material parameters such as the hole effective mass and the band structure consistent with p-type transport in MoS_2.

For each technology (with channel lengths of 16, 32, 65, and 500 nm), we simulate 600 standard cells to obtain statistically significant data. The Monte Carlo engine assigns the device μ_{eff} with a Gaussian distribution mimicking the experimental data of μ_{FE}. Similar Gaussian distributions with CV = 0.1 are assumed for saturation velocity (v_{sat}), R_C, and carrier density variation (s_n). The variation of mobility is independent of channel length because the devices are in the diffusive transport regime[44] and the MoS_2 thickness is the same (monolayer). Variation in threshold voltage V_T is incorporated through the dependence on carrier density variation and EOT scaling with channel length ($s_{V_T} = qs_n/C_{ox}$). To simulate the worst-case scenario, we assume negligible covariance between different inputs.

We quantify the standard cell delays by simulating rise and fall times and define the output rise (fall) time from 10% (90%) of the supply voltage V_{DD} to 90% (10%) of V_{DD}. In Figure 5a, we show a sample of 10 different simulations of rising two-input NAND gate output with 65 nm transistors. For the same standard cell, rise and fall times are extracted from 600 Monte Carlo simulations as shown in Figure 5b. (Additional distributions can be found in Supporting Information Figure S14.) We further quantify the standard cell variation in terms of CV for rise and fall times. As shown in Figure 5c,d, the delay CV < 0.1 for channel lengths down to 16 nm for two-input NAND and two-input NOR gates. This contrasts with other low-dimensional technologies such as carbon nanotubes, where the variation can be significant and requires special processing steps to make useable systems.[46−48]

CONCLUSIONS

In summary, we examined the variability of 2D semiconducting nanofabrics and devices based on CVD-grown monolayer MoS_2. Ultraclean fabrication led to low surface roughness of ~3 Å and surprisingly low variability of key device parameters (such as mobility and threshold voltage) considering the subnanometer thickness of the material. Small variations can come from 1L−2L junctions and grain boundaries, but n-type MoS_2 is naturally immune to these as energy variations are small in its conduction band (~55 meV ~ $2k_BT$ at room temperature). In contrast, conduction band variation in silicon films with comparable thickness is estimated to be ~0.7 eV. Across >1 cm^2 continuous MoS_2 films, the mobility measured by several techniques ranges from 30 to 45 cm^2/V/s (10th to 90th percentile; highest value ~48 cm^2/V/s), and the contact resistance is of the order 1 kΩ·μm at carrier densities >10^{13}

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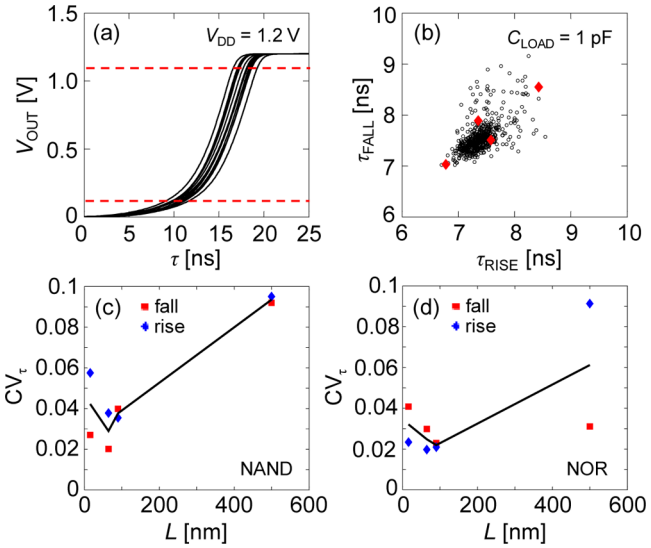

Figure 5. Monte Carlo simulations of standard logic cells using the experimentally measured device variation. (a) Simulated output demonstrating the rise time in two-input NAND gates. We show output waveforms of 10 simulations from over 600 simulations for visual clarity. Red dashed lines represent 10% of V_{DD} and 90% of V_{DD}. (b) Extracted rise times (τ_{rise}) and fall times (τ_{fall}) for 600 NAND gates are shown by black symbols. The performance corners simulated for $\langle\mu_{FE}\rangle \pm 2s_{\mu_{FE}}$ are shown in red diamonds. Additional plots are shown in Supporting Information Figure S14. (c and d) CV in rise times and fall times for NAND and NOR standard cells. The variation in average delay is shown by black lines.

cm^{-2}. These values are among the best obtained to date for undoped monolayer CVD-grown 2D semiconductors. We also used the statistical data as inputs to Monte Carlo simulations to explore how such variations might affect system performance and find the standard cell delay CV < 0.1 for channels down to 16 nm. This study provides key missing steps in the quest to scale 2D semiconductors from materials and devices to realistic system implementations.

METHODS

Growth Procedure. Monolayer (1L) MoS_2 is grown in ~cm^2 films directly on SiO_2/Si substrates by chemical vapor deposition as described in ref 15. In short, 30 μL of 100 μM perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) is decorated around the edges of the HMDS-treated substrate in 2.5 μL droplets and dried on a hot plate. Solid sulfur is loaded into a 2 in. tube furnace upstream of the reaction zone, where the substrate is placed face-down over ~0.5 mg of solid MoO_3. After pumping the tube to base pressure, Ar is used to bring the pressure to 760 Torr before reducing the flow rate to 30 sccm. The furnace is then ramped to 850 °C and held there for 15 min before being allowed to cool back to room temperature.

Device Fabrication and Measurement. All device fabrication is performed in the Stanford Nanofabrication Facility and Stanford Nano Shared Facilities as detailed in Supporting Information section B. Optical lithography is employed to define probe pads, electrical contacts, and channel sizes in three separate steps. O_2 plasma (10 W) is used to etch the MoS_2 away for channel definition before probe pad deposition. Ag/Au is used as a planar contact to the MoS_2 to achieve low contact resistance. Finally, the substrate is loaded into a vacuum probe station (~10^{-5} Torr) and annealed at 250 °C for 2 h, then allowed to cool to room temperature before measurements are performed *in situ*.

Monte Carlo Simulations. A variability model to capture the coefficient of variation of material properties is developed using the experimental data. The Python-based Monte Carlo engine generates 600 samples for each simulation case. The transistors are modeled based on the S2DS model.[45] The circuit simulations are performed using HSPICE, and the data were analyzed using MATLAB.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.7b04100.

Device processing details; additional statistical data; Monte Carlo simulation details (PDF)

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Notes

The authors declare no competing financial interest.

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SUPPORTING INFORMATION

Low Variability in Synthetic Monolayer MoS_2 Devices

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A. Dry thermal SiO_2 on Si (p^{++}) Characterization

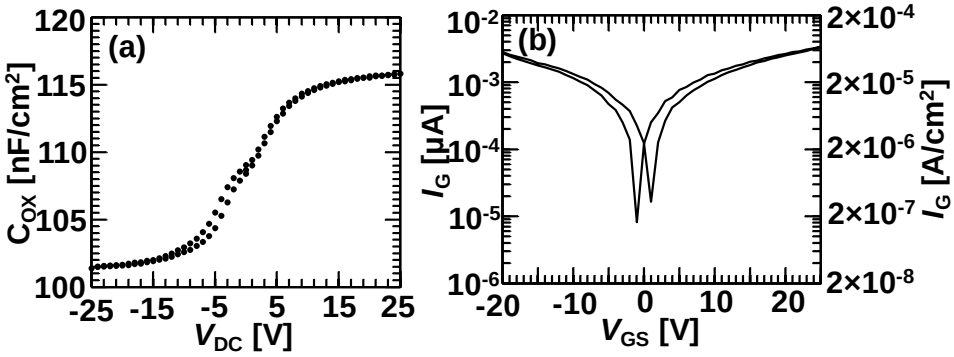

Figure S1. (a) Example C-V measurement (f = 100 kHz, v_{ac} = 30 mV) on a 40 nm Au/1 nm Ti/30 nm SiO_2/500 μm Si (p^{++}) MOScap, normalized to its area. The growing depletion capacitance in the p^{++} Si causes the <10% reduction in the measured capacitance for negative gate biases at this frequency. For V_{DC} > 15 V, the measured capacitance is above 115 nF/cm^2 and approaches the real value C_{ox} ~ 116 nF/cm^2. (b) Measured gate leakage for the same device shown in Figure 1f, both in absolute μA and normalized to the combined source and drain pad area of 5×10^3 μm^2 (also showing forward and backward sweeps). The total leakage remains well below 10^{-4} A/cm^2 for all V_{GS}, and is over four orders of magnitude below I_D at V_{GS} = 25 V. All our oxides are grown in-house at the Stanford Nanofabrication Facility (SNF) using a Thermco oxidation furnace and dry O_2 gas as the oxidant.

B. Process Flow for MoS_2 FET Fabrication and Measurement

All feature definition for this work was performed by optical photolithography using a KarlSuss MA-6 Contact Aligner system (365 nm, 15 mW/cm^2, hard contact mode with a 40 μm gap). For metallization steps, Shipley LOL 2000 was applied (60 s @ 3000 rpm) as a liftoff resist before application of SPR 3612 optical photoresist (PR). For the channel definition, only the latter was used. The two etch steps are done in a Materials Research Corporation model 55 reactive ion etcher (RIE), using 20 sccm O_2 at 10 W and a pressure of 20 mTorr. (We attribute the very small RMS surface roughness of our finished devices to this very gentle etch process.) All metallization steps

were performed in a Kurt J. Lesker electron beam metal evaporator at base pressures of ~5×10^{-8} Torr. (The low pressure of contact evaporation is crucial for good contacts.[S1]) Metal liftoff is done by soaking chips in MicroChem Remover PG at room temperature for at least one hour before spraying with acetone and methanol, and blow-drying with N_2.

The general process flow before measurement is as follows:

1. CVD synthesis of large-area MoS_2 nanofabrics on 30 nm SiO_2 on Si as detailed in Ref. S2.
2. Define probe pads in PR; etch MoS_2 in pad areas; deposit 2/40 nm Ti/Au; liftoff.
3. Define contact regions in PR; deposit 25/25 nm Ag/Au; liftoff.
4. Define channel regions in PR; etch exposed MoS_2; dissolve PR in acetone.
5. Mount chip in a Janis vacuum probe station, pump to pressure of ~2×10^{-5} Torr, and perform a two-hour *in-situ* vacuum anneal at 250 °C followed by an overnight cool-down period.
6. Measure devices *in-situ* at room temperature ~20 °C, in the same vacuum probe station.

C. Additional Statistical Data for V_{DS} = 1.0 V

Measured Quantity	Mean ⟨...⟩	Standard Deviation (s)	α for χ^2 test
Linear V_T	-1.78 V	1.05 V	0.02
Constant-current V_T	-7.42 V	1.79 V	0.46
$\sqrt{I_D}$ V_T	-7.06 V	2.17 V	10^{-5}
Y-function V_T	-0.51 V	0.99 V	0.37
Linear ΔV_T	0.16 V	0.12 V	10^{-3}
n_t	1.1×10^{11} cm^{-2}	0.9×10^{11} cm^{-2}	10^{-3}
$\log_{10}(H)$	-0.8885	0.2246	0.1
$\log_{10}(I_{MAX}/I_{MIN})$	6.6813	0.4015	10^{-7}
μ_{FE}	34.2 cm^2/V/s	3.6 cm^2/V/s	0.13
μ_Y	38.2 cm^2/V/s	4.4 cm^2/V/s	0.34
R_{CY}	3.0 kΩ·μm	0.7 kΩ·μm	10^{-4}
W	11.74 μm	0.13 μm	10^{-21}

Table S1. Means and standard deviations for all values extracted in this study at V_{DS} = 1.0 V. We recall that the V_T here is representative of the t_{ox} = 30 nm oxide thickness. Different equivalent oxide thickness (EOT) will rescale the V_T by the ratio EOT/t_{ox}.

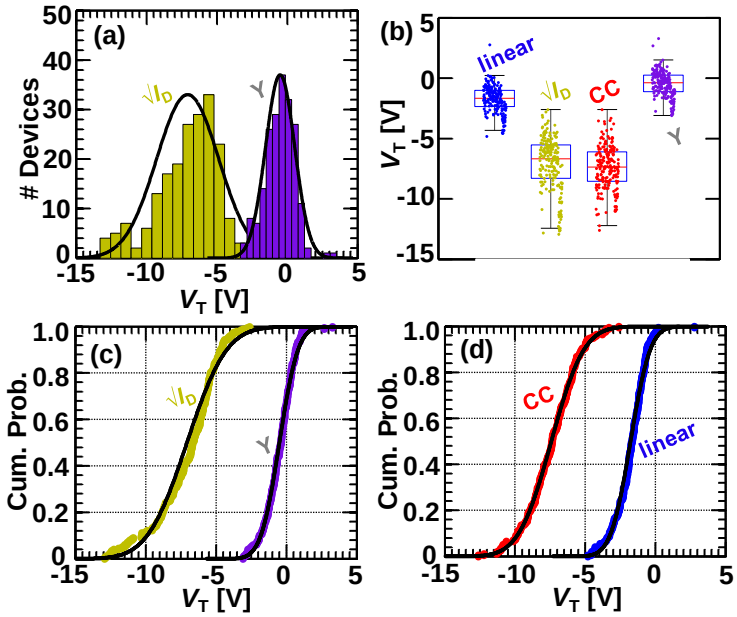

Figure S2. Statistical data representations for different V_T extractions. (a) Histograms and Gaussian fits of V_T extracted by the $\sqrt{I_D}$ (yellow) and Y-function (purple) methods. (b) Box-and-whisker plots of all four extractions, showing that standard deviations for the linear extrapolation and Y-function methods are smaller than those for $\sqrt{I_D}$ and constant-current. (c) Cumulative distribution function (CDF) plots of the same data in (a), with Gaussian fits (black lines). The goodness-of-fit is more easily visualized in this plot. (d) CDF plots of the data shown in Figure 2a.

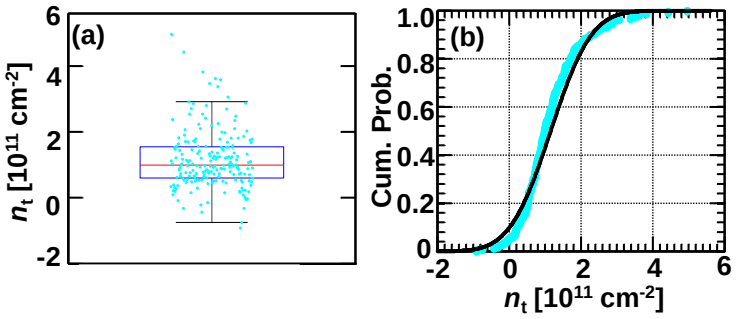

Figure S3. Additional representations of estimated density of charge traps n_t. (a) Box-and-whisker plot, and (b) CDF plot.

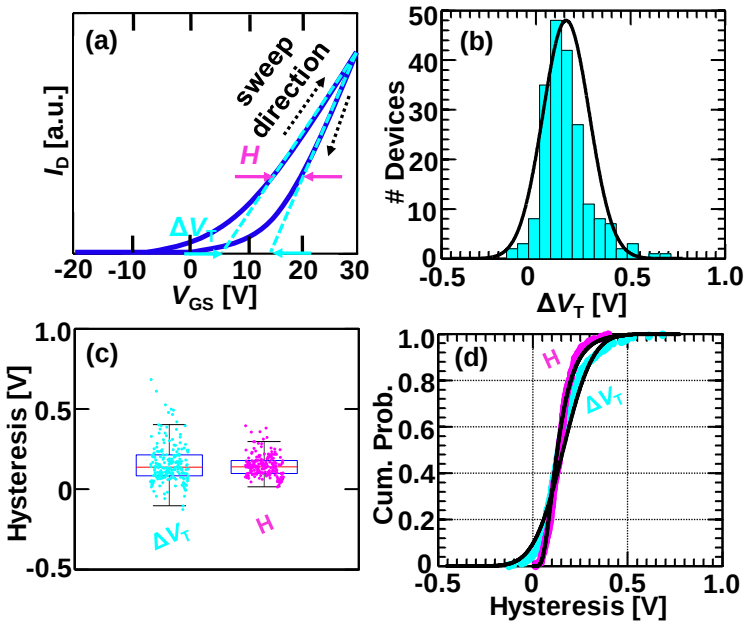

Figure S4. Additional representations of hysteresis extractions. (a) A mock-I_D-V_{GS} sweep with over-exaggerated hysteresis, showing how we extract ΔV_T and H. (b) ΔV_T as measured by linear extrapolation between the forward and backward I_D-V_{GS} sweep. These data correspond directly to Figure 2b of the main text by $n_t = \Delta V_T C_{ox}/q$. (c) Box-and-whisker plots of ΔV_T and the maximum measured hysteresis as taken between all points in the linear region of the forward and backward I_D-V_{GS} sweeps. Given the definitions in (a), it is unsurprising that typical values for H would be less than that for ΔV_T. (d) CDF plots of the same data in (c) along with Gaussian and lognormal fits (lines) for ΔV_T and H, respectively.

It should be pointed out that, despite all values for H being positive as expected, 5% of the extractions for ΔV_T are negative. This is an artifact of the extraction methodology combined with the fact that the hysteresis in our devices is indeed quite small. For any particular extraction of the forward and backward values for V_T, the 95% confidence intervals in the extraction (with the coefficient of determination $r^2 \geq 0.99999$) overlap by 95%. Loosely put, there is a 95% chance that the two values are the same, to 95% certainty in our measurement. This results in the error bars on either side of any one ΔV_T data point in Figures S4b-d being 20–25% greater than the mean value, which would ideally be zero. This highlights the importance of taking measurements on large numbers of data and running statistics. A more strict interpretation of the statistics will only lead to the conclusion that, in addition to ΔV_T being very small, we can only be 95% certain that the population mean $\mu_{\Delta VT}$ is indeed positive. Compare to Figure S11e, where all extractions for ΔV_T and n_t are positive.

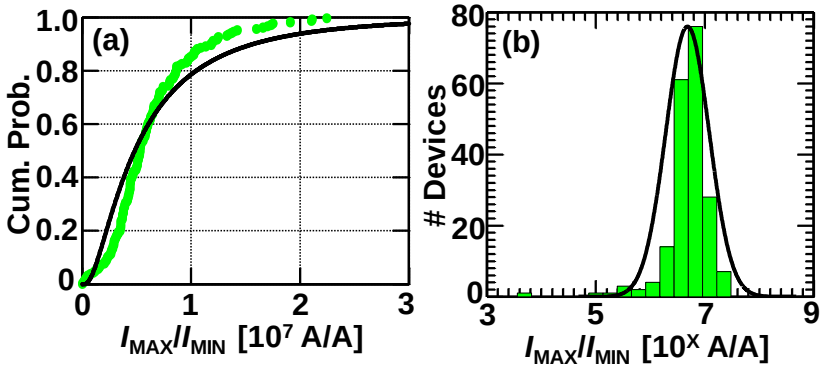

Figure S5. Additional representations of I_{max}/I_{min}. (a) CDF and (b) log-scale histogram plot. We choose the notation I_{max}/I_{min} instead of I_{on}/I_{off} because (1) this is simply the ratio of the highest to lowest measured current for each device, which could be different dependent upon V_T and measurement range of V_{GS}, and (2) on- and off-currents (I_{on}, I_{off}) are set by choosing voltage rails in e.g. a circuit, which we do not have here. Thus the term I_{on}/I_{off} is not well defined in this context.

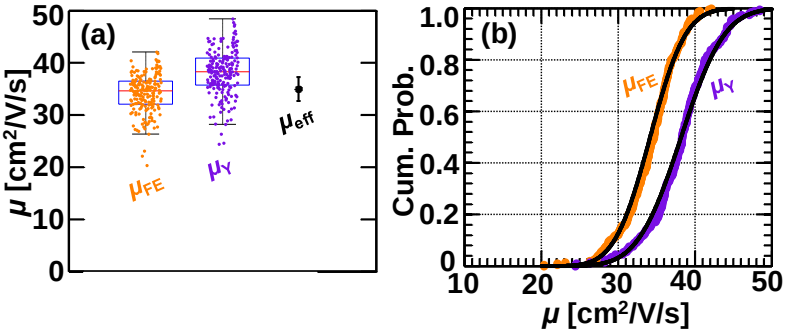

Figure S6. Additional representations of mobility extractions. (a) Box-and-whisker plot showing μ_{FE}, μ_Y, and μ_{eff} from the pTLM with 95% confidence intervals. (b) CDF plots for μ_{FE} (orange) and μ_Y (purple).

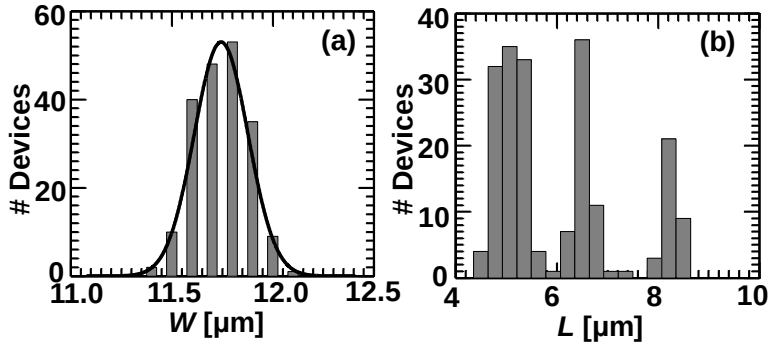

Figure S7. Histograms for geometry values as measured by SEM. (a) W is observed to be Gaussian with a standard deviation of 0.13 µm. (b) The histogram for device lengths L is trimodal since there were three nominal device lengths measured on the chip. Each distribution is itself Gaussian.

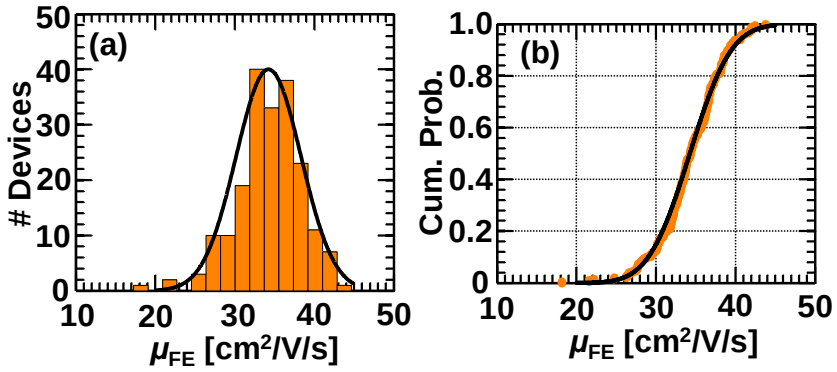

Figure S8. Extractions for μ_{FE} assuming that L and W are their mean values for each device. (a) While the mean is exactly the same, the variance of the histogram for μ_{FE} can be seen to increase slightly with this assumption. The coefficient of variation (CV) only increases slightly due to L and W having such small variances. (b) CDF plot of the data in (a), which may be contrasted to the orange data in Figure S6b.

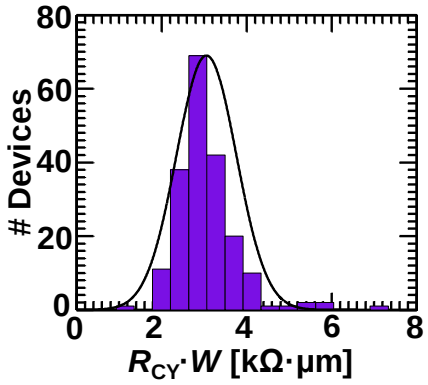

Figure S9. The histogram for R_{CY} shows a mean near 3.0 kΩ·μm.

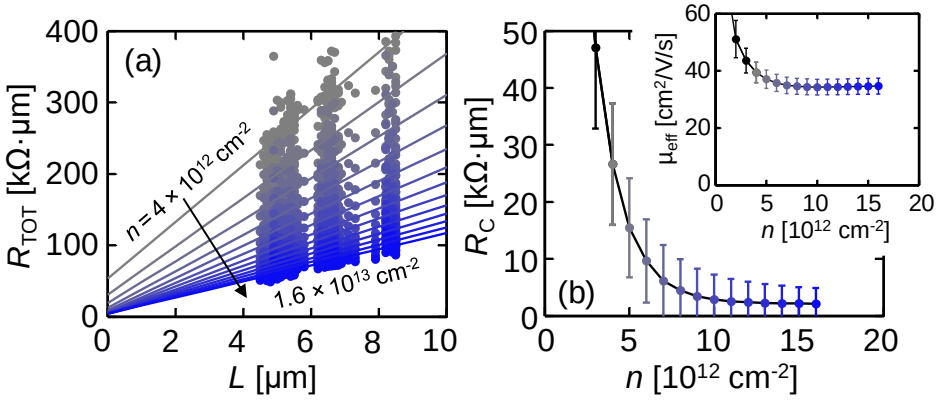

Figure S10. (a) pTLM analysis for V_{DS} = 1.0 V. (b) R_C = 2.1 ± 2.7 kΩ·μm at n = 1.6×10^{13} cm^{-2}. Inset: μ_{eff} = 34.7 ± 2.8 cm^2/V/s. Colors represent increasing carrier density.

D. Additional Statistical Data for V_{DS} = 0.1 V

Measured Quantity	Mean ⟨…⟩	Standard Deviation (s)	α for χ^2 test
Linear V_T	-2.36 V	1.08 V	0.04
Constant-current V_T	-2.06 V	1.56 V	0.02
$\sqrt{I_D}$ V_T	-7.61 V	2.10 V	10^{-3}
Y-function V_T	-1.13 V	1.10 V	0.16
Linear ΔV_T	0.29 V	0.09 V	10^{-4}
n_t	2.1×10^{11} cm^{-2}	0.6×10^{11} cm^{-2}	10^{-4}
$\log_{10}(H)$	-0.6745	0.1305	0.1
$\log_{10}(I_{max}/I_{min})$	5.8623	0.2513	10^{-4}
μ_{FE}	34.4 cm^2/V/s	3.9 cm^2/V/s	0.16
μ_Y	37.8 cm^2/V/s	4.7 cm^2/V/s	0.08
R_{CY}	2.9 kΩ·μm	0.9 kΩ·μm	10^{-7}

Table S2. Means and standard deviations for all values extracted in this study at V_{DS} = 0.1 V. Compare with Table S1 values extracted at V_{DS} = 1.0 V.

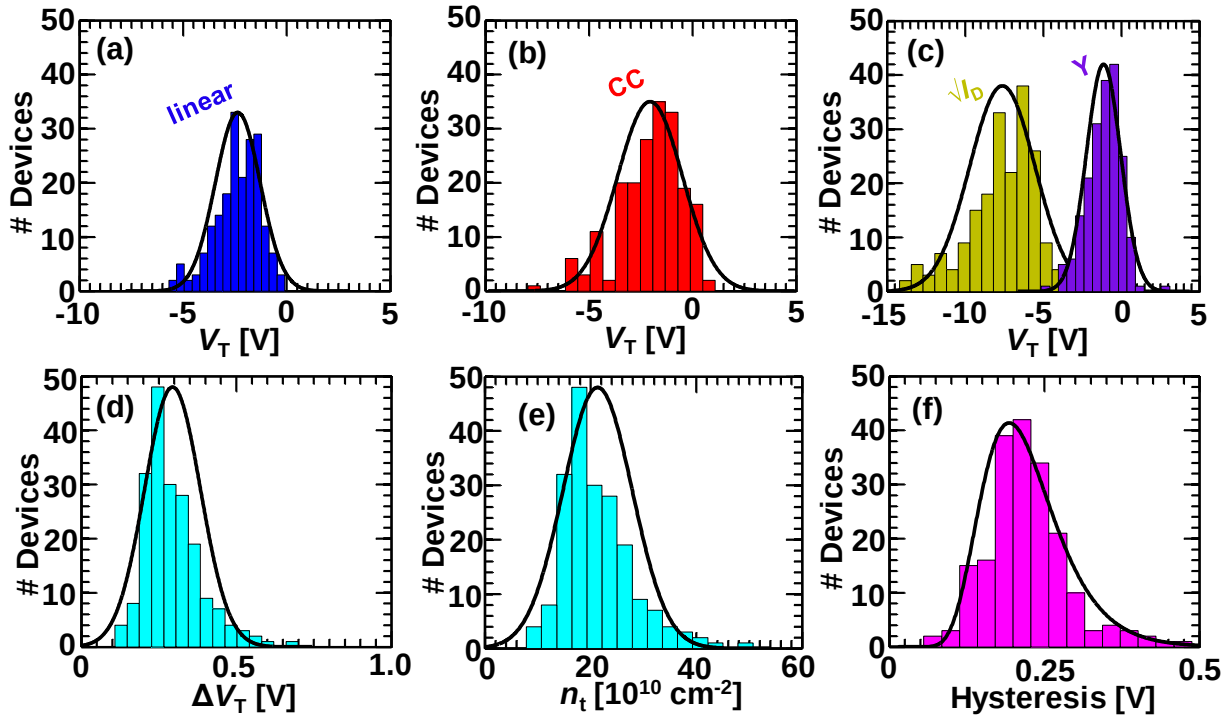

Figure S11. Statistical data representations for the different V_T extractions, ΔV_T, n_t, and H all for V_{DS} = 0.1 V. (a)–(c) Histograms and Gaussian fits of V_T as extracted by the four methods previously mentioned. (d) and (e) ΔV_T and n_t histograms, related by $n_t = \Delta V_T C_{ox}/q$. Note that all values of ΔV_T are positive in this case, as is generally expected. (f) Histogram of measured hysteresis H, which is again lognormal. All values are consistent with those extracted for V_{DS} = 1.0 V in Figure 2.

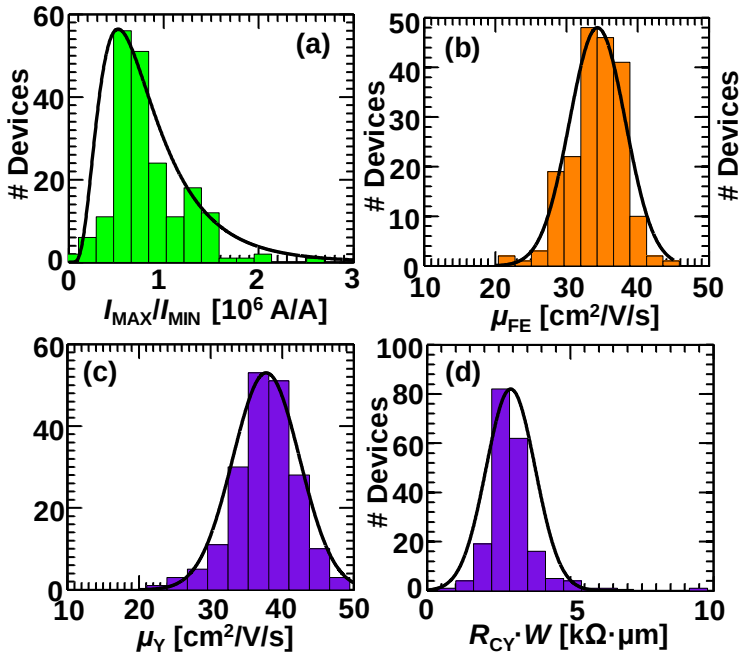

Figure S12. Histograms for V_{DS} = 0.1 V. (a) Histograms and lognormal fit of I_{max}/I_{min}. Note that these values have fallen by approximately one order of magnitude compared to V_{DS} = 1.0 V (see Figure 2d in main text), since these devices are operating in triode and contact resistance is relatively small. (b) μ_{FE} values are again the same as for V_{DS} = 1.0 V (Figure 2e). (c) and (d), mobility and contact resistance as extracted from the Y-function method (compare to Figure 2f at V_{DS} = 1.0 V).

E. Extractions Using the Y-Function Method

As expounded in Ref. S3, mobility can be estimated from the Y-function, $Y = I_D / \sqrt{g_m}$, by the expression $\mu_Y = \left(\frac{Y}{V_{GS} - V_T}\right)^2 \left(\frac{L}{WC_{ox}V_{DS}}\right)$, where V_T is estimated by linear extrapolation from a plot of Y vs. V_{GS} rather than I_D vs. V_{GS}. Further, an upper bound on the minimum single-contact resistance in the strong inversion regime can be estimated by $R_{CY}W \approx \frac{\theta L}{2C_{ox}\mu_Y}$, where θ is a V_{GS}-dependent attenuation factor with units of V^{-1} in the expression $I_D = \frac{\mu_Y}{1+\theta(V_{GS}-V_T)} C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$. From these equations, we calculate μ_Y = 38.2 ± 8.8 cm²/V/s and $R_{CY}W$ = 3.0 ± 1.4 kΩ·μm for V_{DS} = 1.0 V.

F. International Technology Roadmap (ITRS) specifications

In simulations, we optimize the flat band voltage of the top gate (V_{FB}) for each channel length such that the I_{off} (at V_{GS} = 0, V_{DS} = V_{DD}) = 100 nA/μm. Other device parameters used are as per ITRS[S4] specifications as shown in the table below.

L (nm)	t_{ox} (nm)	V_{DD} (V)	R_C (Ω·μm)
16	0.8	0.86	188
32	1.1	1.1	180
65	1.3	1.2	190
500	5.0	3.3	200

Table S3. The device parameters used to simulate MoS_2 transistors with ITRS specifications.[S4]

G. Monte Carlo simulations of standard cells

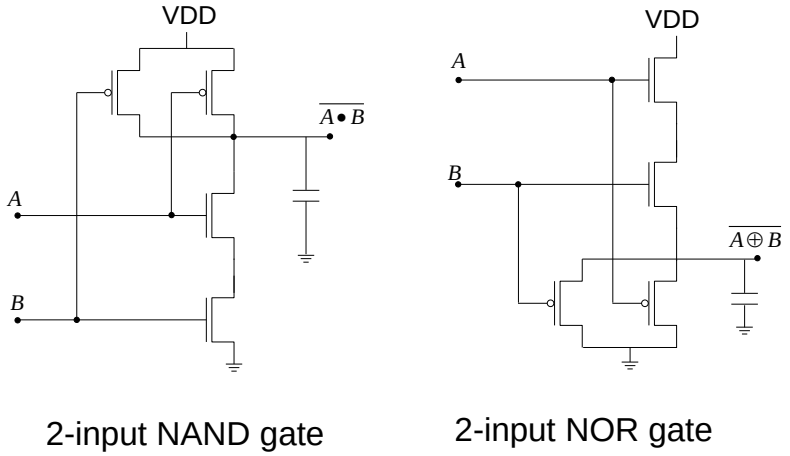

Figure S13. Schematic for 2-input NAND and NOR gate

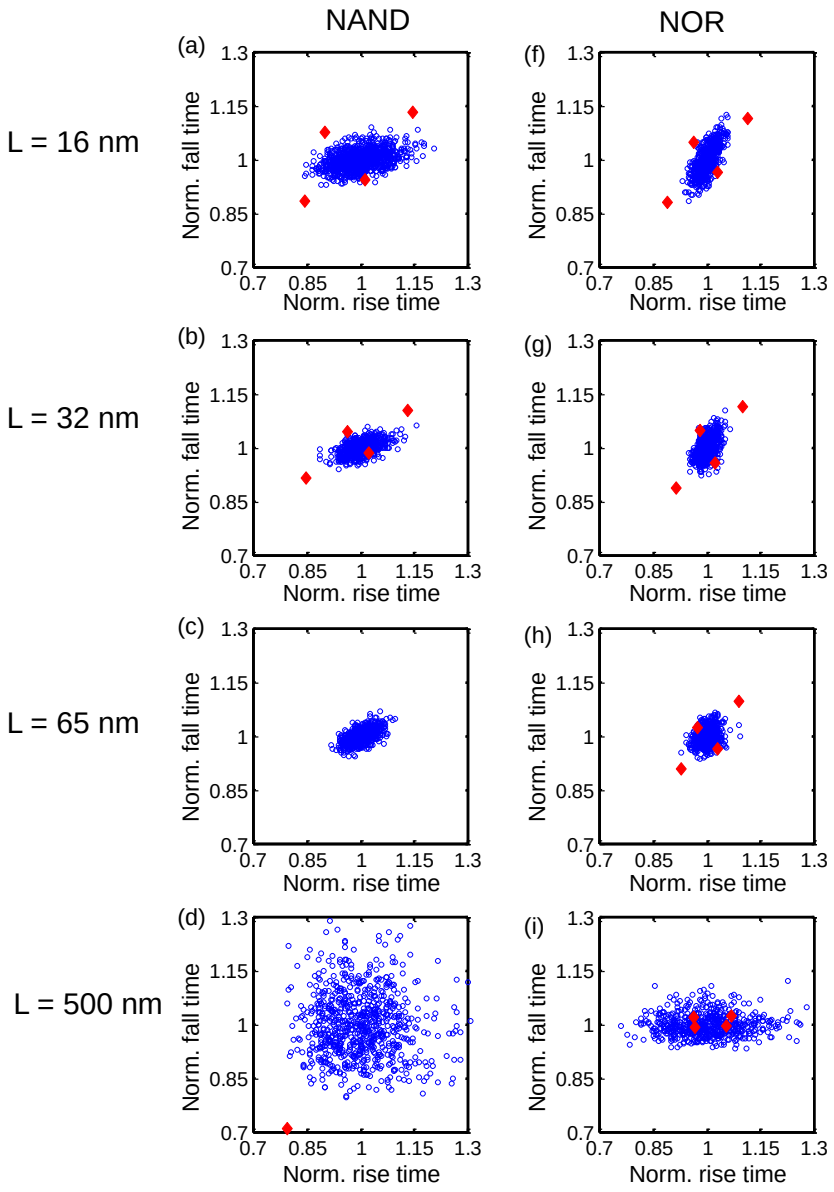

Figure S14. (a) to (f) show Monte Carlo simulations of fall time (τ_{Fall}) and rise time (τ_{Rise}) of NOR2 for 16 nm and 65 nm technology nodes respectively. We have normalized the rise time and fall time for each channel length with respective mean values. The performance corners [NFET-PFET: Fast-Fast (FF), Slow-Slow (SS), Fast-Slow (FS) and Slow-Fast (SF)] are calculated for $\langle \mu_{\text{FE}} \rangle \pm 2s_{\mu\text{FE}}$. The simulated values for the performance corners are shown in red diamonds.

Supplementary References

(S1) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Field-Effect Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16*, 3824–3830.

(S2) Smithe, K. K. H.; English, C. D.; Suryavanshi, S. V; Pop, E. Intrinsic Electrical Transport and Performance Projections of Synthetic Monolayer MoS_2 Devices. *2D Mater.* **2017**, *4*, 011009.

(S3) Chang, H.-Y.; Zhu, W.; Akinwande, D. On the Mobility and Contact Resistance Evaluation for Transistors Based on MoS_2 or Two-Dimensional Semiconducting Atomic Crystals. *Appl. Phys. Lett.* **2014**, *104*, 113504.

(S4) International Technology Roadmap for Semiconductors (ITRS). High Performance (HP) and Low Power (LP) PIDS Tables. URL: <http://www.itrs2.net/itrs-reports.html>.