Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths

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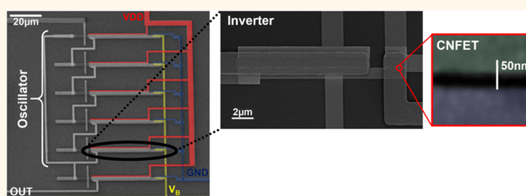
ABSTRACT Carbon nanotube (CNT) field-effect transistors (CNFETs) are a promising emerging technology projected to achieve over an order of magnitude improvement in energy-delay product, a metric of performance and energy efficiency, compared to silicon-based circuits. However, due to substantial imperfections inherent with CNTs, the promise of CNFETs has yet to be fully realized. Techniques to overcome these imperfections have yielded promising results, but thus far only at large technology nodes (1 μm device size). Here we demonstrate the first very large scale integration (VLSI)-compatible approach to realizing CNFET digital circuits at highly scaled technology nodes, with devices ranging from 90 nm to sub-20 nm channel lengths. We demonstrate inverters functioning at 1 MHz and a fully integrated CNFET infrared light sensor and interface circuit at 32 nm channel length. This demonstrates the feasibility of realizing more complex CNFET circuits at highly scaled technology nodes.



KEYWORDS: carbon nanotube · CNT · CNFET · scaling · VLSI · interface circuit

For decades, silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the foundation of the semiconductor industry. While shrinking MOSFET dimensions have traditionally led to higher performance, silicon MOSFETs are becoming increasingly difficult to scale.[1] As the channel length decreases, electrostatic control of the current and mobility in the channel diminishes, limiting the extent to which the devices can scale.[2,3] To further decrease transistor channel lengths and improve performance, alternative transistor materials are being investigated. Single-wall carbon nanotubes (CNTs), nanocylinders composed of a single atomic layer thick sheet of carbon atoms, are a very promising material due to their excellent electrical, thermal, and physical properties.[4,5] CNTs can be used to form CNT field-effect transistors (CNFETs), which, owing to their ultrathin body "thickness" (diameter) of ~1 nm, exhibit excellent electrostatic control and simultaneously high mobility.[6,7] Due to these device-level benefits, it is projected that CNFET-based digital systems can achieve over an order of magnitude improvement in energy-delay product, a metric of performance and energy efficiency, compared to competing technologies.[8,9]

Additionally, CNTs are promising candidates as sensors in a wide range of applications,[10] due to their exceptionally high surface-area-to-volume ratio, and much work has been dedicated toward developing novel CNT sensors.[11−13] As the need for low-power electronic systems expands, CNTs are also one potential energy-efficient alternative for the sensor interface circuitry, especially when implemented in a digitally oriented topology.[14] Therefore, there are additional applications of using CNFETs to develop highly energy-efficient integrated sensor and interface circuits.

There has been significant progress made toward realizing high-performance CNFET-based digital systems. Since the first initial demonstrations of CNFETs,[16,17] much effort has been invested in demonstrating high-performance individual CNFETs, and recent results have even achieved aggressively scaled 9 nm channel lengths.[18] While these impressive stand-alone, single-CNT devices have shown the capability of CNFETs to scale beyond traditional bulk MOSFETs, questions remain concerning the feasibility of fabricating integrated digital systems

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using CNFETs. Substantial imperfections inherent to CNT technologies, such as metallic and mis-positioned CNTs, have prohibited circuit demonstrations using these highly scaled CNFETs in the past.[19] Mis-positioned CNTs cause erroneous connections in a circuit, while metallic CNTs (m-CNTs) decrease on/off current ratios (I_{on}/I_{off}), both resulting in increased leakage power and incorrect logic functionality.

To overcome these inherent imperfections, earlier work has developed the imperfection-immune design paradigm.[20] The imperfection-immune design paradigm is a set of very large scale integration (VLSI)-compatible design and processing techniques that overcome both the presence of mis-positioned and m-CNTs within a circuit in a scalable manner. Using the imperfection-immune design methodology, larger-scale CNFET digital systems were made possible, resulting in experimental demonstrations of CNFET circuits ranging from stand-alone logic elements, such as half-adder sum generators and D-latches[21] to a CNFET interface circuit for a non-CNT-based sensor,[14,15] to the first demonstration of a basic CNT computer.[22] However, these demonstrations were limited to the 1 μm technology node, and questions remained as to whether these imperfection-immune techniques could scale to smaller technology nodes.

In this work we present the first VLSI-compatible approach to realizing CNFET digital circuits at highly scaled technology nodes, with channel lengths ranging from 90 nm to sub-20 nm. We show inverters fabricated in our VLSI-compatible approach at these scaled channel lengths operating at 1 MHz. Moreover, as CNTs are also promising candidates to act as sensors in a range of applications, we also demonstrate a fully integrated CNFET infrared (IR) light sensor and interface circuit with 32 nm channel length CNFETs. With the ability to scale to smaller technology nodes, our VLSI-compatible circuits obtain major improvements in operating frequency (~100×) and power consumption (~2500×) compared to previous CNFET-based sensor interface work.[14] This work therefore demonstrates the feasibility of realizing more complex CNFET circuits at highly scaled technology nodes.

RESULTS AND DISCUSSION

Overcoming Imperfections. We show that the imperfection-immune design paradigm[20] can overcome both mis-positioned and m-CNTs at sub-20 nm channel lengths. To overcome mis-positioned CNTs, we begin with chemical vapor deposition (CVD) growth of highly aligned CNTs at a wafer scale.[23] This is accomplished by performing the growth on a crystalline quartz substrate, resulting in CNTs growing along the crystalline grooves of the substrate,[24] with 99.5% CNTs aligned.[23] To address the remaining mis-positioned CNTs, we employ mis-positioned-CNT-immune design,[25] which is a layout technique whereby predefined regions of a wafer are etched out, removing any CNTs within that region. The etch regions are defined within the standard cells of the library and guarantee that if any mis-positioned CNT could have caused incorrect logic functionality, part of the CNT must travel through an etch region and would be removed. It has been shown previously that mis-positioned-CNT-immune design can be applied to any logic function and follows VLSI design and processing flows, as there is no per-unit customization.[25] Given that mis-positioned-CNT-immune design is a layout technique, it is effective regardless of scaling, and we use it later in our fabrication of the sensor interface circuit.

Ideally, CNT growths should yield pure semiconducting CNTs (s-CNTs). However, this is currently not feasible, as even the most optimized CVD growths yield 2−5% m-CNTs,[26,27] while typical growths can result in up to 33% m-CNTs.[28] There have been several techniques demonstrated for removing m-CNTs post-growth, ranging from selective gas etching of m-CNTs[29] to solution-based sorting,[30] thermocapillary flow followed by etching of m-CNTs,[31] and electrical breakdown of m-CNTs.[32] While several of the above techniques have yielded exciting results,[33,34] electrical breakdown has shown the ability to remove >99.99% of all m-CNTs, the necessary selectivity for VLSI-scale application.[35] To perform electrical breakdown, s-CNTs are turned "off" by a back-gate, and a source−drain voltage is applied across the device. As the s-CNTs are off, only the m-CNTs conduct current, and by applying a sufficiently large source−drain voltage, the m-CNTs break down through a Joule self-heating process.[36]

However, selective electrical breakdown of m-CNTs has only been previously applied to devices with channel lengths of 1 μm.[22,35] As channel length decreases, several changes occur: diminished gate control due to short-channel effects[37] decreases the ability to turn off s-CNTs; in addition, the source and drain could act as heat sinks as the CNT length decreases,[38] resulting in the inability for the m-CNTs to reach breakdown temperature. To determine the feasibility of performing selective m-CNT electrical breakdown on highly scaled channel lengths, we use a local back-gate device geometry, with a high-κ gate dielectric (HfO_2) with effective oxide thickness (EOT) of ~4.25 nm. This approach gives devices the necessary control to turn off s-CNTs during electrical breakdown. We show that we can perform electrical breakdown on channel lengths ranging from 1 μm to sub-20 nm, increasing I_{on}/I_{off} ratios from initially ~1−2 (due to the presence of m-CNTs) to >10^4 after removing all m-CNTs (Figure 1). Additionally, as channel length scales, I_{on} increases both pre- and post-electrical breakdown (Figure 1 and Supporting Information). As shown in Figure 1, as the channel length is reduced, the required breakdown voltage (V_{BD}) also decreases, while the breakdown *power* per unit length remains approximately constant.[38]

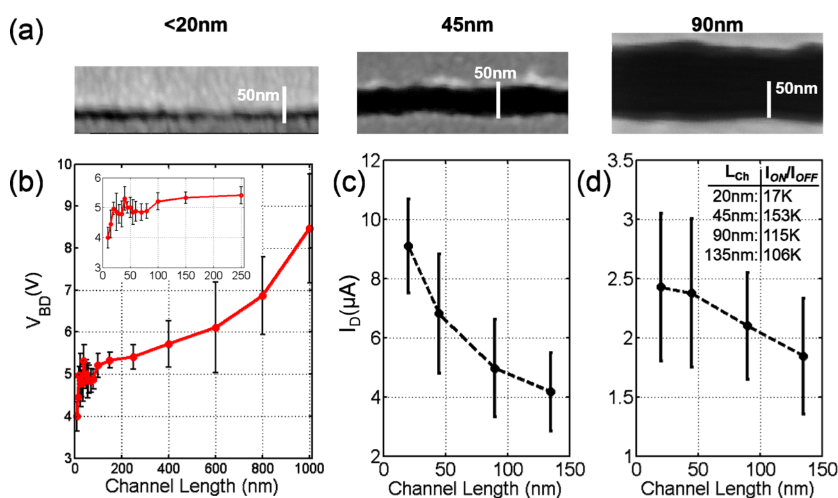

Figure 1. (a) Scanning electron microscopy (SEM) of devices with channel lengths of <20 to 90 nm. (Individual CNTs are not always visible in SEM.) Electrical breakdown was performed on CNFETs with channel lengths spanning from <20 to 1 μm. (b) Average measured breakdown voltages for CNFETs over a range of channel lengths. Error bars show 90% confidence interval. As the channel length scales, the required breakdown voltage decreases. The inset shows an expanded view of channel lengths below 250 nm. (c) Average initial I_{ON} versus channel length, before electrical breakdown. Error bars show 90% confidence interval. As channel length scales, I_{ON} increases. (d) Average final I_{ON} versus channel length, after electrical breakdown. Error bars show 90% confidence interval. Average I_{ON}/I_{OFF} after electrical breakdown for each channel length is shown in the table in the top right. As channel length scales down, I_{ON} increases.

As a result of lower V_{BD}, thinner back-gate dielectrics can be used without the risk of dielectric breakdown, in turn enabling electrical breakdown of m-CNTs while maintaining gate control of the s-CNTs at these scaled technology nodes.

Simulations of m-CNT breakdown were performed using COMSOL, with device geometries closely matching our fabricated devices. For CNTs shorter than a few hundred nanometers, the axial thermal conductance can approach ballistic limits even at elevated temperatures characteristic of breakdown in air (~600 °C) due to long phonon mean free paths. In order to capture this behavior within our simulations, we employ a temperature (T)- and length (L)-dependent thermal conductivity model of the CNT inspired by a recent study of quasi-ballistic heat flow in graphene[39] and fit to high-temperature data available for CNTs:[40]

$$k(L,T) = \left[3.4 \times 10^{-7}T + 9.4 \times 10^{-10}T^2 + 2.3T^{-2} + \frac{1}{[G_{\text{ball}}(T)/A]L}\right]^{-1}$$

where $G_{\text{ball}}(T)/A \approx [1/(4.4 \times 10^5\, T^{1.68}) + 1/(1.2 \times 10^{10})]^{-1}$ W K^{-1} m^{-2} is a polynomial fit to the ballistic thermal conductance per cross-sectional area (A) of graphene,[39] which is identical for CNTs at nearly all temperatures of interest (*e.g.*, $T > 50$ K).[41] The electrical resistance was calculated following the quasi-ballistic model introduced by ref 36:

$$R(V,T) = R_C + \frac{h}{4q^2}\left[1 + \int_{-L/2}^{L/2} \frac{dx}{\lambda_{\text{eff}}(V, T(x))}\right]$$

where q is the elementary charge, h is the Planck constant, λ_{eff} is the electron mean free path, and R_C is the electrical contact resistance.[36] The electrical contact resistance between the CNT and the metal contact (20 nm Pt) is taken as $R_C \approx 10$ kΩ in series with the quantum contact resistance ($h/4q^2 = 6.5$ kΩ), which is included in the expression above. (We note that changes in R_C do not radically alter our thermal simulation results, only shifting them up or down slightly.) The thermal boundary resistance between the CNT and metal contacts is ~10^{-8} m^2 K W^{-1}, and the thermal conductance between the CNT and substrate is 0.14 W K^{-1} m^{-1} at room temperature, increasing to 0.2 W K^{-1} m^{-1} at the breakdown temperature.[36,42] The contact area in both cases is taken as half the CNT circumference multiplied by the length of the contact region, which assumes that the bottom half of the CNT is in contact with the substrate while the top half is in contact with the metal contacts.

In the simulation, the source–drain channel separation was varied over a range from $L = 10$ nm to 1 μm. To obtain the V_{BD} at each technology node, steady-state simulations were run with applied source–drain voltages ranging from 3 to 5 V in 200 mV increments, and the maximum temperature was recorded. The V_{BD} was interpolated as the voltage at which the maximum temperature along the CNT reached $T_{BD} \approx 600$ °C, the temperature required for breakdown in air.[42–44] Figure 2 shows the expected V_{BD} *versus* channel length L, revealing the same trend of requiring less breakdown voltage as the devices scale (experimentally measured in Figure 1).

Additionally, due to the high thermal conductance and extremely small thermal volume of individual CNTs, transient-response simulations reveal that CNTs reach their breakdown temperature extremely rapidly,

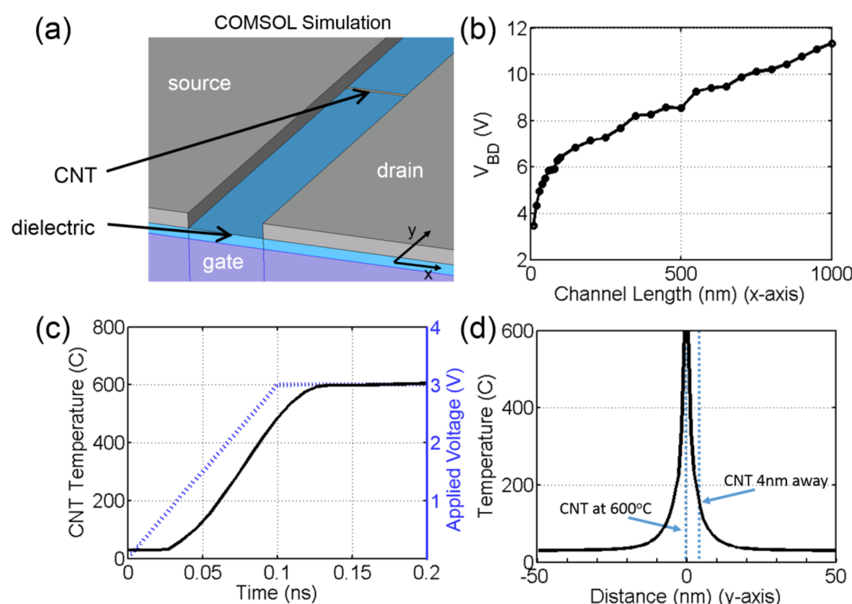

Figure 2. (a) COMSOL simulation setup. The source and drain are Pt, the dielectric is HfO_2, and the gate is Si. (b) Expected breakdown voltage *versus* channel length from COMSOL simulations. Good agreement with experimental results shown in Figure 1(b). (c) Simulated transient breakdown response of CNTs (L = 20 nm). The linear ramp is the applied voltage, with the temperature increase slightly lagging behind due to heat capacitive effects. (d) Computed temperature profile between two CNTs separated by 4 nm, when the left-hand CNT at x = 0 reaches ~600 °C breakdown temperature. The right-hand CNT is only at ~150 °C (L = 20 nm).

within less than 0.1 ns, consistent with molecular dynamics simulations.[45] To confirm this experimentally, a pulse unit was used to apply variable pulse widths to break down the CNTs, ranging in widths from 100 ns to <5 ns (time pulse seen by CNTs less than applied pulse width due to capacitive charging of the wires). Pulses of <5 ns were sufficiently long to break down the CNTs. The application of nanosecond pulses also mitigates unwanted dc biasing effects across the thin dielectrics, *e.g.*, charge trapping, hysteresis, and premature dielectric breakdown. With close agreement between our COMSOL and experimental results, we further use the COMSOL model to investigate the proximity effect of CNT breakdown between adjacent CNTs.

Additional questions have been raised concerning the scalability of electrical breakdown to high (~200 CNTs/μm) CNT densities, *i.e.*, whether the breakdown of a m-CNT would cause local heating of adjacent CNTs spaced 4–5 nm apart, causing these CNTs to also break down, irrespective of whether they are semiconducting or metallic. In the simulation, a source–drain voltage is applied to heat the CNT to 600 °C, its breakdown temperature, and another CNT is placed 4 nm away. The steady-state temperature profile is shown in Figure 2d, which shows one CNT at 600 °C, while the other CNT 4 nm away remains at ~150 °C. Therefore, our simulation results together with our experiments demonstrate that electrical breakdown can both scale to ~20 nm channel lengths and remain effective with high (~200 CNTs/μm) CNT densities.

After performing electrical breakdown using local back-gated devices, we show that we can form back-gate, top-gate, and dual-gate CNFETs, of both p- and n-type, demonstrating the flexibility of our technique (Figure 3).[46–48] As the breakdown is already performed with the local back-gate, the top-gate dielectric does not need to withstand the larger breakdown voltage, but only the voltages used during circuit operation. Thus the top-gate dielectric can be further scaled in thickness to allow for better device performance and is fabricated with an EOT of ~2.5 nm. This results in increased performance using the dual-gate structure (Figure 3). Therefore the m-CNT removal process is amenable with more advanced device geometries for further increased performance.

Implementation. We use the above techniques to demonstrate CNFET circuits scaled from 90 nm to sub-20 nm channel lengths, fabricated in a VLSI-compatible manner. The fabrication process is similar to that previously described by Shulaker *et al.*,[49] but two additional electron-beam lithography exposures and metal depositions are used to pattern extended sources and drains to decrease the channel length to the desired value (Figure 4) (detailed process steps are discussed in the Methods section). While electron-beam lithography is the only non-VLSI-compatible process step, this is only a limitation of performing fabrication in an academic fabrication facility. For any technology scaled to sub-20 nm channel lengths, the lithography must be able to pattern at such dimensions, and any adequate lithography technique could replace our electron-beam step. To remove the m-CNTs, we use the electrical breakdown technique described above. However, to keep the entire process

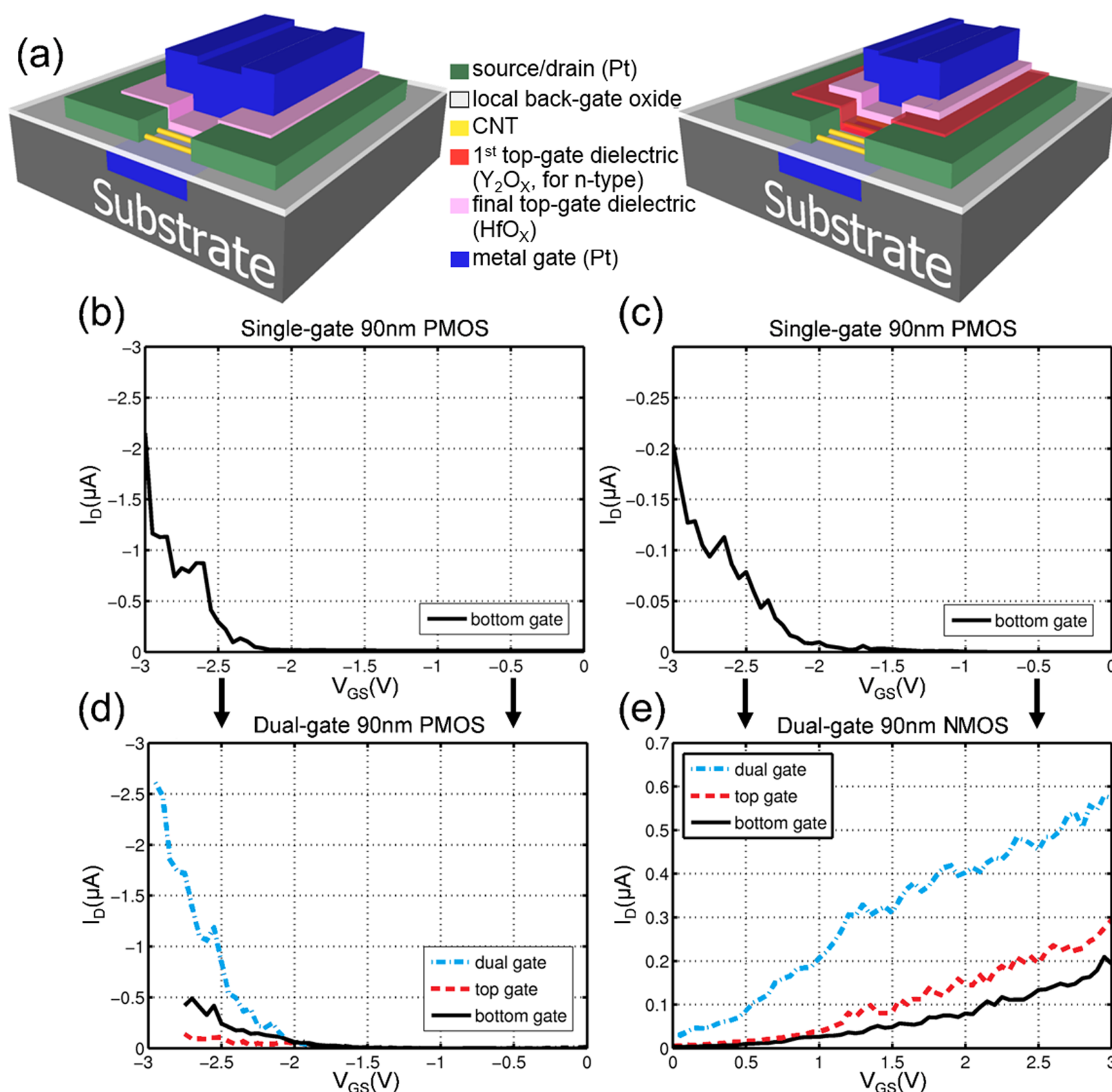

Figure 3. Complementary dual-gate CNFET structures and measured *I*−*V* characteristics, showing bottom-, top-, and dual-gate structures after m-CNT removal. (a) Schematics of CNFETs. PMOS is on the left, NMOS is on the right. (b, c) With only local back-gate, both CNFETs are p-type. (d, e) Through the top-gate deposition, the CNFETs are modified to be either n-type or p-type. The dual-gate CNFETs have increased electrostatic gate control compared to only the local back-gate.

VLSI-compatible, we employ VMR (VLSI-compatible metallic CNT removal).[35] VMR is a design technique allowing electrical breakdown to be performed at the chip level rather than on individual CNFETs, rendering the electrical breakdown process VLSI-compatible. A sacrificial layer of metal is used to connect every source, drain, and gate together, forming a single large device composed of all CNFETs in parallel. This VMR structure, composed of all CNFETs, undergoes electrical breakdown all at once, followed by selectively etching the unneeded metal wires used for the one-time breakdown step.

CNFET Circuits. To demonstrate VLSI-compatible CNFET circuits, we have implemented a fully integrated 32 nm channel length CNFET-based IR light sensor and interface circuit. Sensor interface circuits are ideal applications for CNT technology, as they require low power and high energy efficiency. The circuit implemented here is a time-based sensor interface that processes the sensor information in the time domain. Converting the sensor information to, and processing it in, the time domain allows for greater energy efficiency, due to the fact that the circuits can be implemented in a highly digital manner, resulting in low power and scalable designs.[14,50] The interface circuit consists of two building blocks: a sensor-to-period converter and a period-to-digital converter. Cascading these two building blocks results in a full sensor-to-digital converter (Figure 5). The sensor-to-period converter is implemented as a five-stage sensor-controlled inverter-based ring oscillator, with the IR sensor integrated in the oscillator itself. The IR-to-period converter works as follows: when a CNFET is exposed to IR light, the drive current of the CNFET increases[51] (Figure 7). Therefore, when the CNFET-based oscillator is exposed to IR light, each stage drives more current, increasing the oscillation frequency. The period of the oscillator is

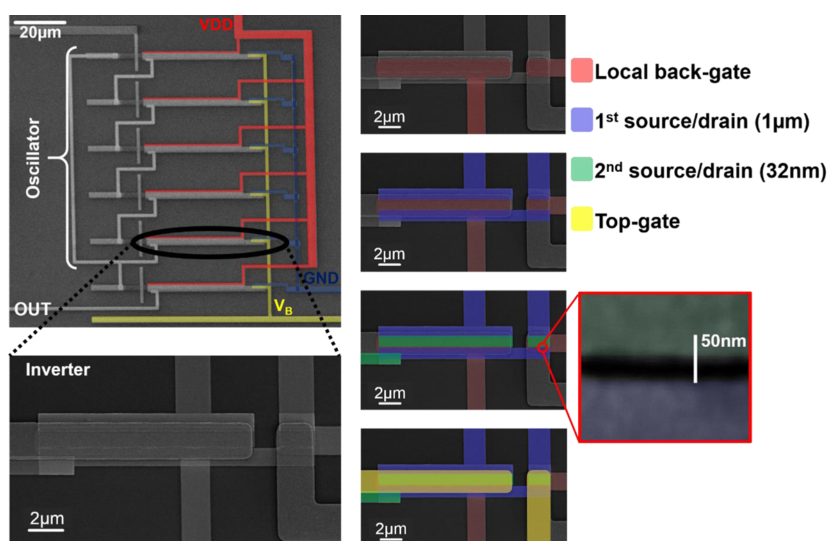

Figure 4. Scanning electron microscopy of an integrated CNFET IR sensor and interface circuit, along with processing steps. The first lithography step defines 1 μm channel lengths, followed by two source–drain extensions (defined through aligned electron-beam lithography) to form 32 nm channel lengths. Detailed process steps are discussed in the Methods.

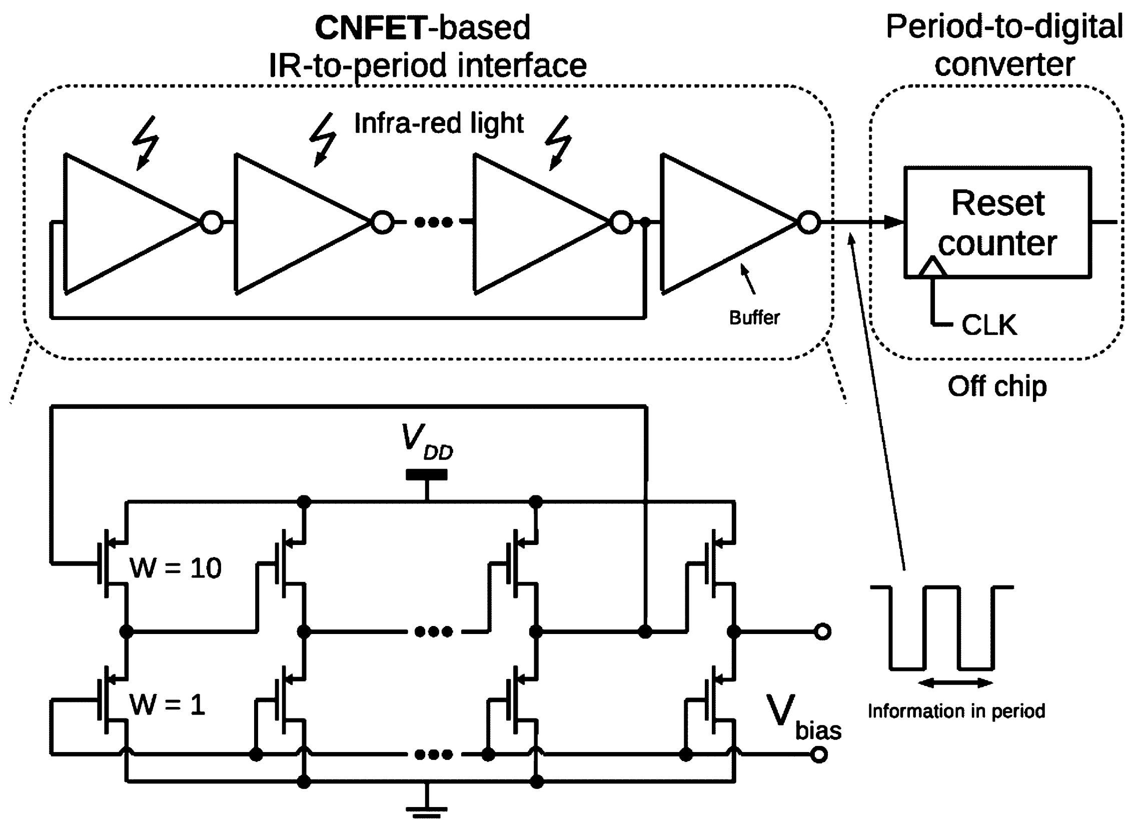

Figure 5. Circuit schematic of the integrated CNFET-based IR sensor and sensor interface. It consists of two blocks: a sensor-to-period converter and a period-to-digital converter. The sensor-to-period converter is implemented entirely with CNFETs as a five-stage sensor-controlled inverter-based ring oscillator, with the IR sensor integrated in the oscillator itself.

thus dependent on the intensity of the IR light, which means that the sensor-to-period interface circuit itself acts as the IR sensor. In addition, the output of the five-stage oscillator is buffered through an extra inverter to read the signal off-chip without loading the oscillator. The implementation is thus entirely digital, which makes this interface highly scalable to implement. Measurements have been carried out with an active probe to minimize loading on the output buffer (see Methods for more details).

After the sensor information is converted to a period-modulated signal, the period can easily be

digitized by a simple reset counter and a decimator.[52] These oscillator-based quantizers exhibit similar behavior to $\Delta\Sigma$ modulators. Due to the quantization error integration, the error is first-order noise-shaped.[52] Due to this quantization noise-shaping effect, the interface benefits significantly from oversampling.[53] As a result, a single-bit quantization (single-bit counter) is sufficient for conversion with moderate resolution. This

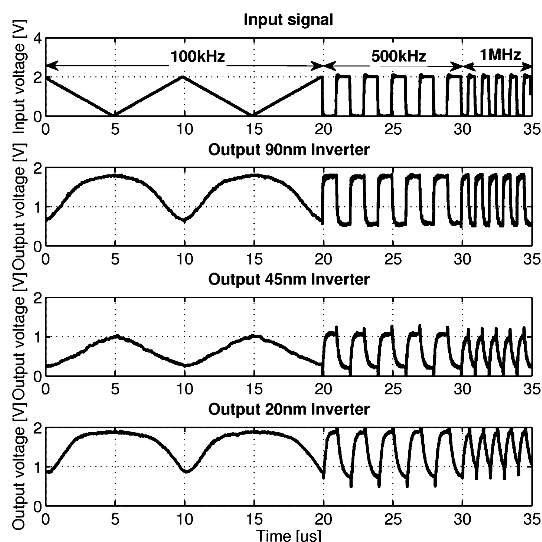

Figure 6. Inverters fabricated in a VLSI-compatible approach, with channel lengths from sub-20 to 90 nm operating at 100 kHz, 500 kHz, and 1 MHz.

means that the reset counter in the period-to-digital converter from Figure 5 is limited in depth to a single bit. In our implementation, the reset counter is implemented off-chip, while the core of the interface, the sensor-to-period converter, is implemented entirely with CNFETs on-chip.

The basic building blocks of the sensor and interface circuit are inverters. As the inverters must be sensitive to IR light, they use only p-type local backgate structures, as top gates would reflect any IR light. Measurement results of individual inverters with channel lengths of 90, 45, and sub-20 nm are shown in Figure 6, operating at speeds up to 1 MHz. Further speed-up requires additional device-level improvements, such as improved contact resistance and increased CNT density; previous work has shown promising techniques for overcoming these obstacles.[49,54] Figure 7 shows the measurement results of the complete sensor interface system from Figure 5. The entire circuit is composed of ~1000 individual CNTs. Measurements show that without IR light the oscillation frequency is ~100 kHz. When illuminated with IR light (880 nm wavelength, 100 mW power), the oscillation frequency increases to ~115 kHz. The difference in output swing is due to the changing relative sizing between the pull-up and pull-down CNFETs in the inverters under illumination, as I_{on} and I_{off} of the CNFETs are affected differently by the IR light (Figure 7). The circuit operates with a scaled-down supply voltage[14] of 2 V, while V_{bias} = −1 V, consuming only ~130 nW of power. This is a major improvement in both

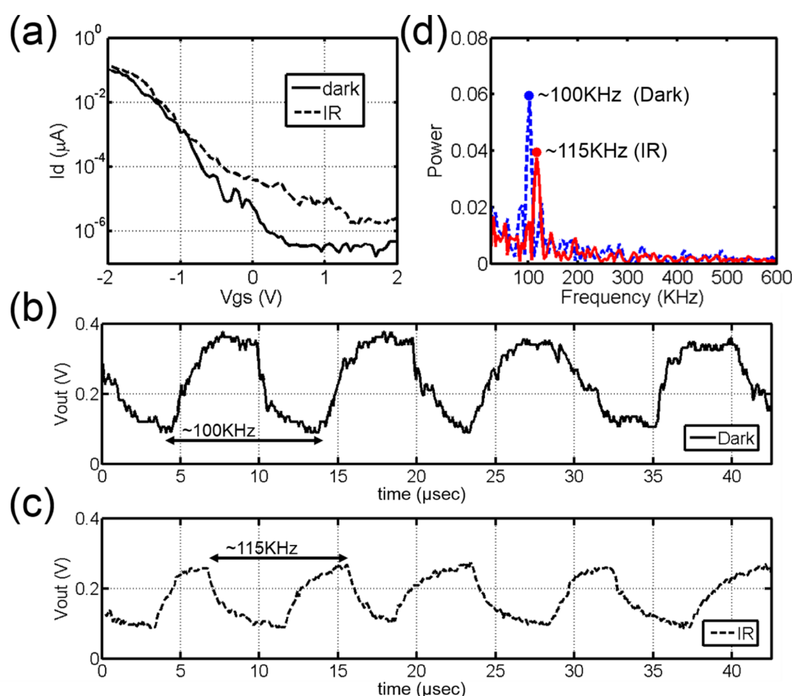

Figure 7. (a) CNFET current dependence on IR illumination. Drive current increases under IR illumination (b, c) The interface circuit responds to the IR light by increasing the oscillation frequency. In (b), the CNFET ring oscillator oscillates in the dark at ~100 kHz. In (c), the CNFET ring oscillator is under IR illumination, and the oscillation frequency increases to ~115 kHz. (d) Power spectrum density for the CNFET ring oscillator from (b) and (c), showing resonant peaks at ~100 and ~115 kHz, respectively.

the operating frequency and the power consumption compared to prior work. Compared to a previous CNFET-based sensor interface at the 1 μm technology node, we achieve a 100× speed improvement and a 2500× power consumption improvement.[14]

CONCLUSIONS

We have demonstrated the first VLSI-compatible highly-scaled CNFET circuit. The circuit demonstrated is a 32 nm channel length fully integrated CNFET sensor and interface system, operating at ~100 kHz while consuming only 130 nW at 2 V supply voltage. We have also demonstrated the subcomponent circuit blocks operating in the MHz regime. We have experimentally shown that m-CNT removal can scale to sub-20 nm channel lengths, allowing for these circuit demonstrations to be performed in a VLSI-compatible manner. Detailed simulations corroborated by experimental data support that electrical breakdown can be a scalable process, in terms of both decreasing channel length and increasing CNT density. Moreover, we have shown that the process is amenable to more advanced device geometries, demonstrating complementary dual-gate CNFETs after m-CNT removal. This work therefore has demonstrated the feasibility of realizing more complex CNFET circuits at highly scaled technology nodes. To next fully realize the energy efficiency and performance of scaled CNFET circuits, additional obstacles, such as increasing CNT density and improving contact resistance, must be overcome. There have been promising demonstrations of approaches capable of overcoming these obstacles,[19,49,54,55] which together with this work bring us one step closer to realizing the exciting potential of highly scaled CNFET circuits as a digital VLSI technology.

METHODS

CNT Growth. ST-cut quartz is used for aligned CNT growth and is initially annealed at 900 °C in a hydrogen ambient. Following anneal, iron catalyst is evaporated (nominally ~3 Å thick) in patterned striped regions across the wafer, forming parallel catalyst stripes 4 μm wide and 200 μm apart. The CNTs are grown at 865 °C with methane feedstock gas.[23]

Transfer. Following growth, the CNTs are transferred to a traditional SiO_2/Si substrate for circuit fabrication. The transfer process is well documented[49] and involves first depositing 150 nm gold on the quartz wafer. The gold is removed from the quartz with thermal release tape and is aligned and placed onto the target substrate. The wafer is heated to 120 °C to remove the thermal release tape, and the gold is etched away in a wet etch the CNTs are inert to. This leaves the CNTs on the target substrate, maintaining both the alignment and density of the grown CNTs.[23]

Device Fabrication. Initial circuit fabrication was patterned with a traditional stepper with a minimum resolution of ~500 nm. The local back gates of the transistors with high-*k* dielectrics, connecting wires, and sources and drains (channel length 1 μm) were fabricated wafer-scale, shown in Figure 4. Following the circuit fabrication, extended source and drain contacts (Pt) were defined with electron-beam lithography. Platinum is used due to its ease of lift-off. Both contacts had to be extended, because line edge roughness of the initial lithography of the stepper was greater than the minimum channel lengths. The two extended metal layers were patterned and deposited separately. The source was initially extended on all devices 100 nm into the channel. Following source definition, the drains were patterned with increasing extensions into the channel. For an 800 nm channel, the drain would extend 100 nm into the channel; for a 50 nm channel, the drain would extended an additional 850 nm. For extremely small channel lengths, the drain extension was stepped by 5 nm, due to offsets in alignment. Scanning electron microscopy was used to calibrate the expected channel length to the actual channel length. Following final channel definition, mis-positioned CNTs were etched with an oxygen plasma following mis-positioned CNT-immune design, and electrical breakdown was performed to remove the metallic CNTs. Electrical breakdown was performed on the final highly scaled devices, with channel lengths ranging from sub-20 nm to 1 μm.

Measurements. To determine the breakdown voltage required for varying channel lengths, dc electrical breakdown was performed. The gate of the transistor was biased off, and the source−drain voltage was swept from 0 V until breakdown was complete. Final I_D-V_{GS} sweeps would confirm whether all metallic CNTs had been removed from the device, achieving I_{on}/I_{off} ratios of $>10^4$. As the devices had more than a single CNT, current was measured while sweeping the breakdown voltage, and breakdown of individual CNTs can be seen as discrete jumps in decreasing current during the sweep. Current changes of >3 μA was used as the threshold for breakdown to exclude erroneous noise.

For inverter and circuit measurements, an active probe was used to minimize loading of the output buffer. A Picoprobe model 12C was used from GGB Industries for probing the 25 μm square probe pad on the wafer, with 2 MΩ input resistance and 0.1 pF input capacitance.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Additional discussion on scaling properties of electrical breakdown and I_D-V_{GS} of typical devices both pre- and post- electrical breakdown. This information is available free of charge *via* the Internet at http://pubs.acs.org.

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