AVALANCHE-INDUCED CURRENT ENHANCEMENT IN SEMICONDUCTING SINGLE-WALLED CARBON NANOTUBES

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THESIS

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ABSTRACT

In this study, semiconducting single-wall carbon nanotubes under high electric field stress (~10 V/μm) are found to display a remarkable current increase due to avalanche generation of free electrons and holes. Unlike in other materials, the avalanche process in such 1D quantum wires involves access to the third subband and is insensitive to temperature, but strongly dependent on diameter ~exp(-1/d^2). Comparison with a theoretical model yields a novel approach to obtain the inelastic optical phonon emission length, $\lambda_{OP,ems} \approx 15d$ nm. The combined results underscore the importance of multiband transport in 1D molecular wires. Finally, based upon the results, carbon nanotubes are shown to be good candidates in avalanche-driven devices with highly nonlinear characteristics.

To my parents for always fostering my love of science and engineering

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CHAPTER 1
INTRODUCTION

1.1 MOS Transistor Scaling Issues

For reasons of both performance and economics, transistor scaling has been the driving force behind the success of the semiconductor industry. Scaling down the size of transistors has allowed for faster processor speeds and increased the physical volume output of transistors. However, as technology continues to advance, it marches toward a brick wall of physical limitations.

1.1.1 Static Power Dissipation and Subthreshold Slope

The most daunting task in CMOS scaling is the problem of power dissipation. As transistors continue to shrink, the power density has increased exponentially as seen in Figure 1.1. There are two main contributors to power dissipation: dynamic power and leakage power. Dynamic power P_{dyn} is power used in switching devices on and off and is given by $P_{dyn} = fC_LV_{DD}^2$, where f is the clock frequency, C_L is the load capacitance, and V_{DD} is the supply voltage. Leakage power P_{leak} is power that is dissipated through current leakage paths in the device and is given by $P_{leak} = I_{leak}V_{DD}$.

The bigger of the two contributors is the leakage power because it is power that is not being used for computation and is contributing to power dissipation both when the device is and is not being used. Scaling has only served to compound the problem as once insignificant leakage paths such as gate leakage become increasingly significant. One such contributor to leakage that has reached its physical limitations is the static subthreshold leakage current. The subthreshold leakage current scales as $exp(-V_T/S)$, where V_T is the threshold voltage and S is the subthreshold slope. If the subthreshold slope could be lowered, then leakage current and power would be lowered as well.

In current MOSFETs, the subthreshold current under diffusive transport is thermodynamically limited to ~k_BT/q = 60 mV/dec. Current technologies are already just barely above that limit and are not improving. The general form of the subthreshold current is

$$I_D = I_{D0} \exp\left(\frac{qV_{GS}}{nk_BT}\right) \tag{1.1}$$

where $n \geq 1$[1]. If Eq. (1.1) is expanded and then S is subsequently derived (dV_{GS}/dI_D), the result is the thermodynamic limit of k_BT/q. Of course, this assumes that the subthreshold current slope is linear. If it were to become nonlinear, then a smaller S may be obtained.

1.2 Impact Ionization

1.2.1 Basic Impact Ionization Physics

Impact ionization (II) is a phenomenon that has been studied for a long time in current semiconductor technologies. The phenomenon comes about when a carrier, either an electron or a hole, is accelerated by an electric field. The further the carrier travels, the more energy it gains. Eventually it must relax its energy and must go somewhere. If the carrier energy at the time of relaxation is greater than the band gap E_g of the material, then that lost energy may be compensated by exciting an electron from the valence band into the conduction band, creating an electron-hole pair (EHP). The process is depicted in Figure 1.2 showing EHP generated in a parabolic band [2]. From the description, it should be expected that the minimum electric field required to accelerate a carrier for II, known as the breakdown field F_{th}, will vary with E_g. From the literature [3], the value for F_{th} is plotted against E_g for various semiconducting materials in Figure 1.3, and indeed a strong dependence is shown.

The probability of a carrier undergoing II was derived by Shockley in 1961 through his lucky electron model [4]. In this model, Shockley determines that the only way a carrier will impact-ionize is if it is accelerated over some distance E_{th}/qF, where E_{th} is the impact ionization threshold energy and F is the applied electric field. However, if the carrier releases its energy to emit a phonon after some mean free path (MFP) λ, then its energy will be lost and thus II would not occur. The lucky electron model thus derives the probability for II, P_{II}, as

$$P_{II} = \exp\left(-\frac{E_{th}}{qF\lambda}\right) \tag{1.2}$$

In most cases the value for E_{th} will be close to that of E_g. Thus it can be seen from Eq. (1.2) that in order to achieve the same P_{II}, the field must scale with the E_g, which matches with what is seen in Figure 1.3, where F_{TH} vs. E_g is plotted for various semiconductor materials.

1.2.2 Impact Ionization in Semiconductor Devices

The benefits of semiconductor devices come from their ability to modulate the electric field within the semiconductor very precisely. This control over the electric field under normal operating circumstances allows for carrier transport to be controlled in some desired form. However, there are circumstances where the precise control can be lost. Cases where the device deviates from a desired state of operation but is not physically harmed are known as "soft" breakdowns. Sometimes, the device will undergo what is known as a "hard" breakdown where the device is physically and permanently damaged.

Impact ionization has long been described as a mechanism that causes a soft breakdown. When the field, whether it is in a p-n junction or a metal-semiconductor

interface, inside a device is made so high that II can occur, carrier multiplication becomes possible. That is to say, an EHP that is created from II goes on to impact-ionize, creating subsequently more EHPs. This sudden influx of carriers causes a sudden up-kick in current, as can be seen for the case of the MOSFET in Figure 1.4 [5]. The phenomenon is known as avalanche breakdown. If the device is kept in the avalanche regime and the current is allowed to increase, then the soft breakdown will eventually turn into a hard breakdown as the device heats up from joule heating and eventually burns out. It is for this reason that II has traditionally been viewed as an undesirable effect in devices.

1.2.3 I-MOS

As mentioned in Section 1.1.1 the subthreshold slope in a MOSFET is limited to 60 mV/dec. One proposed device to beat the subthreshold limit is the impact ionization MOS (I-MOS) [6]. The I-MOS uses nonlinearity generated from impact ionization to increase the subthreshold slope. An I-MOS is essentially a gated p-i-n diode as shown in Figure 1.5A. The device is biased constantly just below the breakdown regime in the off-state and is biased in the breakdown regime in the on-state. Bringing the device into and out of the breakdown regime is achieved by modulating the effective channel length in the intrinsic region. At low gate bias, there is no inversion layer, making the whole intrinsic length the effective channel length. At higher gate biases, an inversion layer is created, thus shrinking the effective channel length to L_I. When the effective length suddenly shrinks while a constant voltage bias is applied between source and drain, the effective field will increase. This puts the device into the breakdown regime and causes a sharp increase in current. Figure 1.5B shows simulations performed by Gopalakrishnan [6], demonstrating a possible subthreshold slope of 5 mV/dec.

While an innovative idea, the I-MOS is not without its shortcomings that need to be solved. Of course with a device biased in the breakdown regime, questions about reliability are a big concern. Even if we can use the device reliably, current experimental results have yet to bring down the operating voltage of the I-MOS to where it would be practical [7, 8]. One adjustable parameter is the semiconductor material. As previously mentioned, the breakdown field in a semiconductor depends upon the band gap of the material. If the bandgap is very small, then the breakdown field should be small as well. However, if E_G is too small then mechanisms such as band-to-band tunneling may dominate transport.

1.3 Carbon Nanotubes

Carbon nanotubes (CNTs) are the cylinder form of the carbon allotrope family. Other carbon allotropes include such materials as diamond, graphite, graphene, and fullerenes. Example images from a scanning electron microscope (SEM) and optical microscope are shown in Figure 1.6. The structure of carbon nanotubes is best described by first studying graphene. Graphene is a monolayer-thick sheet of carbon atoms. The carbon atoms are bonded to each other through sp^2 bonds to form a hexagonal honeycomb lattice. When that sheet is a cylinder, it is called a CNT. Since their discovery by Iijima [9], carbon nanotubes have become a hot topic of research. Single-walled nanotubes (SWNTs) have diameters of roughly 0.5–4 nm, which qualifies them as a one-dimensional system. Multiwalled nanotubes (MWNTs) are nanotubes with one or more additional coaxial cylinder shell. These structures are often considered to be two- or three-dimensional. All nanotubes have very interesting properties because of their honeycomb lattice. They have extremely high electrical ($\sim 100 \times \sigma_{Cu}$) and thermal ($\sim 5 \times k_{Cu}$)

conductivity. In addition, they are mechanically flexible yet hard to break. All of these outstanding properties have given rise to many proposed applications from transistors to space elevators.

1.3.1 Carbon Nanotube Electronic Band Properties

Again, it is useful to first understand properties of graphene in order to explain those of nanotubes. Through tight binding calculations, the band structure of graphene is shown in Figure 1.7 [10]. Graphene contains six Dirac points. There is no energy gap, so this gives graphene metal-like electronic properties. However, because of its Dirac points the carrier population in graphene can be modulated by changing the Fermi level, just like a semiconductor. In addition, around the Dirac points, the bands are symmetrically linear and the electron dispersion relation can be given as $E(k)=\hbar v_F k$, where v_F is the Fermi velocity. The symmetry between the conduction and valence bands means that both electrons and holes will have the same effective mass and will hence have the same mobility.

The band structure for CNTs is very similar to that of graphene. Essentially, a nanotube is a rolled up sheet of graphene. The band structure will change depending on how the nanotube is "rolled." As part of the graphene is rolled up into a nanotube, some of the energy states in graphene are cut out. If the Dirac point is not cut, then the nanotube is considered to be metallic. If the Dirac point is cut and the bands separate as a result, then the nanotube is considered to be semiconducting. Since different rolling angles will cut off different graphene energy states, the band separation will vary with the rolling angle, shown in Figure 1.8 [11]. Generally, one third of carbon nanotubes should end up being metallic and two thirds being semiconducting based on all the available

rolling angles. How much of the graphene sheet is used determines the diameter of the tube, which will dictate what states are cut out. Larger diameter tubes will retain more states from graphene, so they will tend to have smaller E_G. Kataura has calculated the relationship between energy separations of carbon nanotube bands and subbands and his result is plotted in Figure 1.9 [12]. The relationship between E_G and nanotube diameter d can be approximated as $E_G \sim 0.84/d$.

1.3.2 Electronic Transport in Single Walled Carbon Nanotubes

SWNTs are considered to be one-dimensional conductors of electricity. Their small diameter and even smaller thickness quantize transport along the length of the tube. Because of their 1-D nature, nanotubes are often thought of as 1-D quantum wires. Using a Landauer model, it is possible to calculate the ballistic limit of conductance in SWNTs. Landauer's formula for calculating current through a 1-D channel is given as

$$I = \frac{2e}{h}\int_{\mu_1}^{\mu_2} g(E)f(E)T(E)dE \tag{1.3}$$

where $g(E)$ is the density of states (DOS), $f(E)$ is the Fermi distribution function, $T(E)$ is the transmission probability, and μ_1 and μ_2 are Fermi levels of channels 1 and 2, respectively. In the ballistic case T=1, the best conductance, taking into account both sub-band and spin degeneracy, is given as

$$G = \frac{4e^2}{h} \tag{1.4}$$

Experimental results have come very close to reaching this quantum limit in very short, submicron-long carbon nanotubes, where defects are minimized and optical and acoustic phonon scattering do not play a minimal role as shown by Javey et al. in Figure 1.10 [13].

As the nanotube lengthens, so does the number of mechanisms that cause scattering, thus further limiting carrier transport. Nanotubes in this length regime are said to have diffusive transport. There are experimental restrictions such as atomic defects, kinks, and surface roughness that can act as scattering points for carriers traveling through the nanotube [14]. Furthermore, physical mechanisms provide more restrictions to carrier transport through nanotubes. At least in metallic nanotubes, it has been shown that optical phonon scattering and Joule heating limit the current through a nanotube to the range of 20–25 μA [15, 16]. The current limit in semiconducting SWNTs was thought to be similar, but till now had not been studied very thoroughly. This thesis will show how, through II [17], the currents in a semiconducting SWNT can well exceed the 25 μA current limit.

1.3.3 Carbon Nanotube Field Effect Transistors

Because carbon nanotubes have very high mobility, even in diffusive samples [18], they are promising candidates for post-Moore's-law transistors. The most commonly fabricated carbon nanotube field effect transistor (CNTFET) in research labs is a back-gated CNTFET, shown in figure 1.11. More details on the structure will be given in chapter 2. In a CNTFET, the nanotube serves as the channel for conduction with a highly doped substrate serving as the back gate. These devices are naturally p-type. In order to gain better electrostatic control in the channel, top-gates may be added by depositing a layer of dielectric material on top of the nanotube and then subsequently adding an electrode on top [19]. For the purpose of this study, bottom gated CNTFETs were sufficient. Future work however, possibly to emulate the I-MOS, could require use of a top-gate.

1.4 Figures

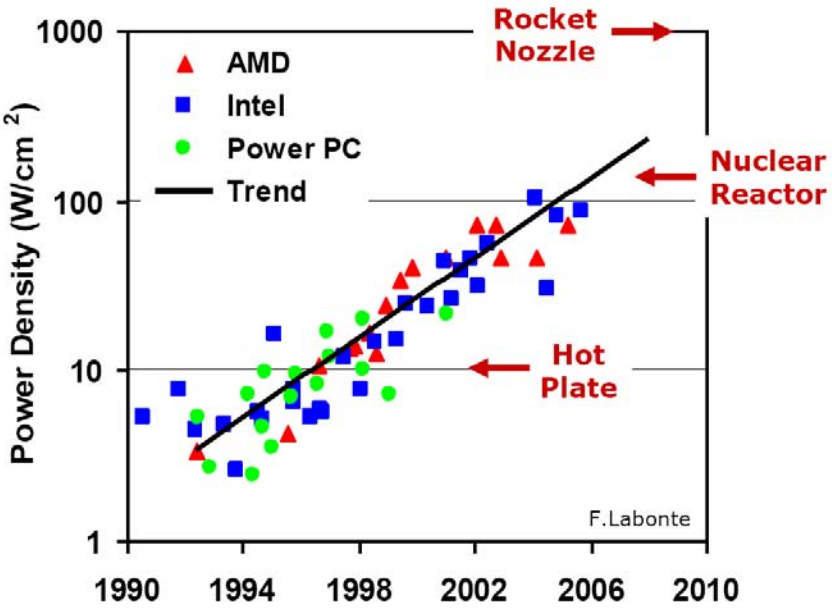

Figure 1.1: Power density of devices surveyed from AMD, Intel, and Power PC. Continuation of the current trend will lead to processors that will not be able to survive the heat generated from power densities of continued scaling.

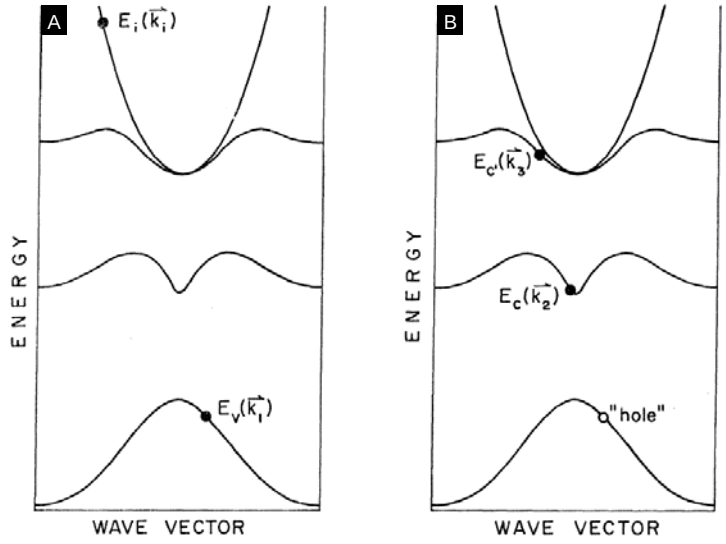

Figure 1.2: Impact ionization depicted in a generic E vs. k diagram of an electron (A) before impact ionization and (B) after impact ionization generating an electron hole pair [2].

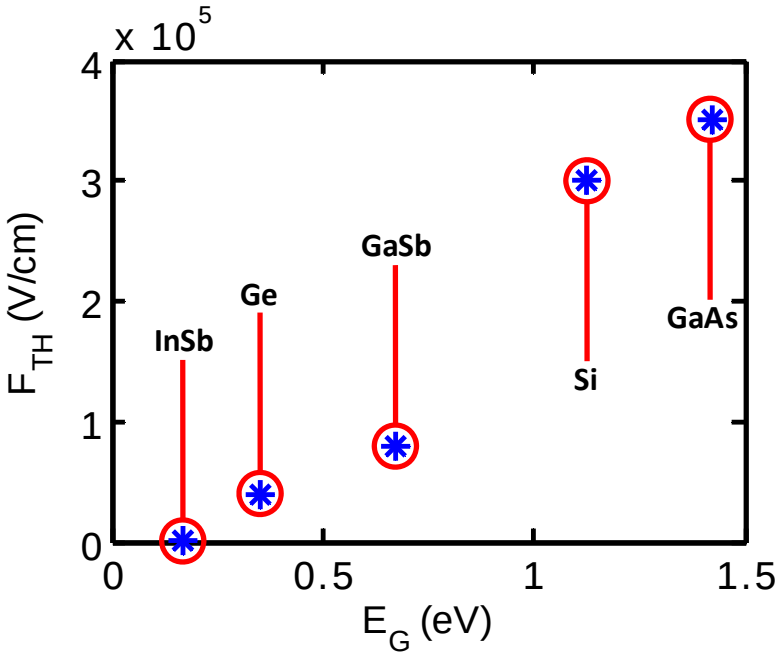

Figure 1.3: Avalanche breakdown field as a function of energy gap for Si, Ge, GaAs, InAs, and InSb.

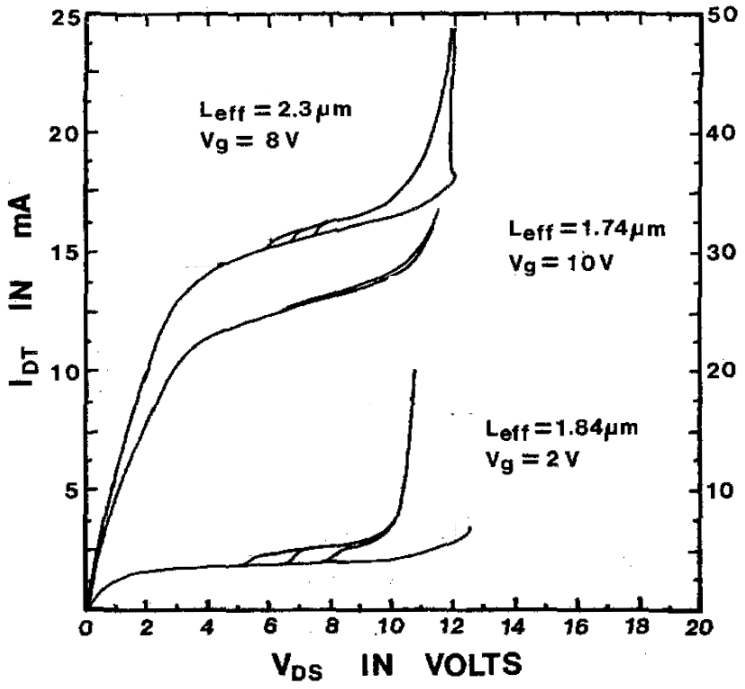

Figure 1.4: Typical avalanche breakdown in MOSFETs measured at different gate biases, showing the current suddenly increasing at high bias [5].

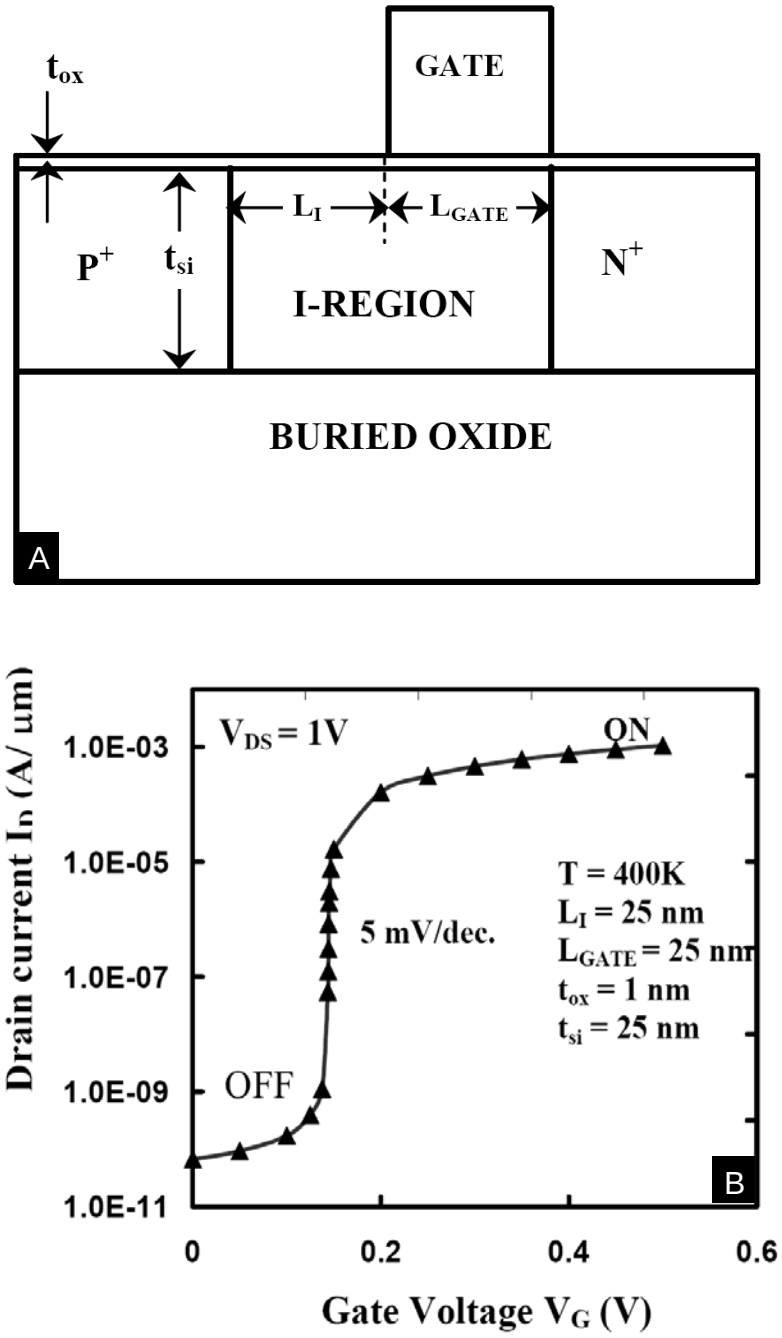

Figure 1.5: (A) Cross section of a typical I-MOS. The gate is used to control the effective channel length and thus modulate the maximum field strength in the channel. (B) Simulated transfer characteristics for an I-MOS showing a subthreshold slope of 5 mV/dec [6].

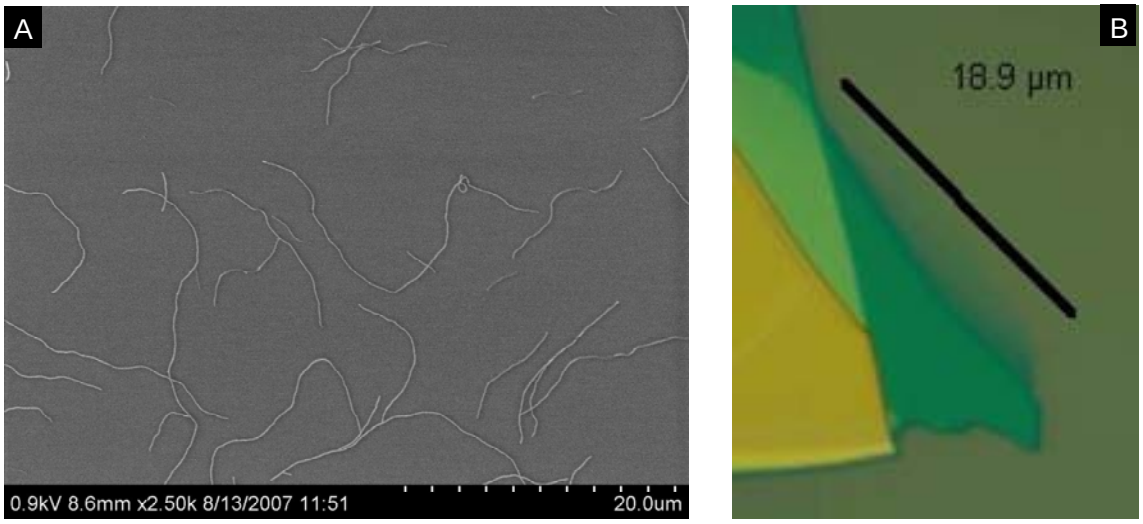

Figure 1.6: (A) Scanning electron microscope of randomly grown carbon nanotubes. (B) Optical image of graphene. Lighter areas indicate fewer layers.

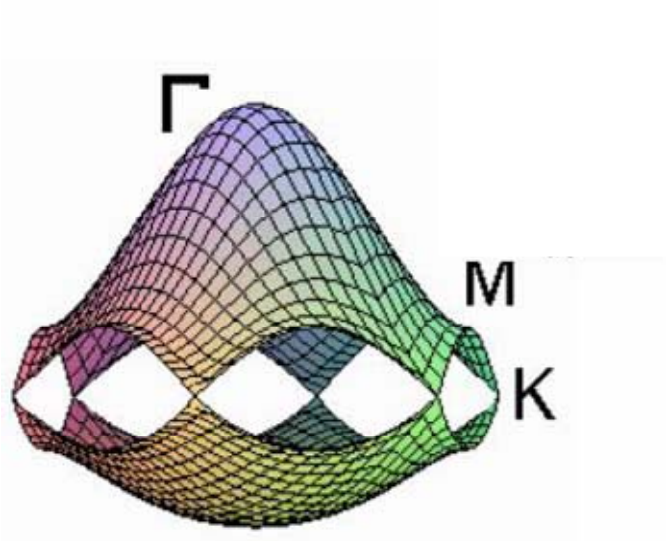

Figure 1.7: The 3-D band structure of graphene showing six Dirac points and linear dispersion about those points [10].

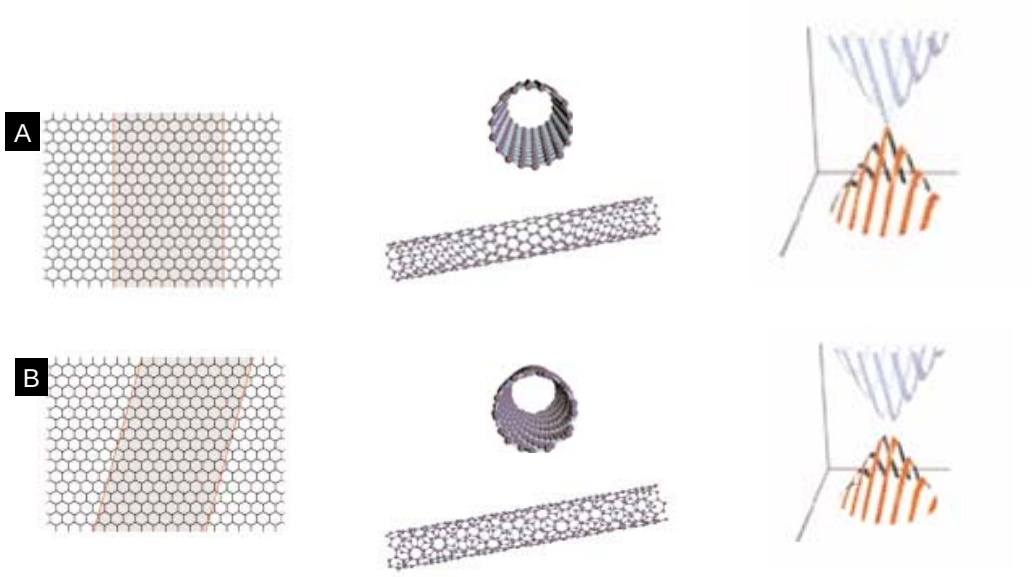

Figure 1.8: The left column shows a graphene sheet and the area that is rolled up to form a nanotube. The middle column shows the subsequent SWNT produced. The right column shows the energy states that are cut off by the nanotube with (A) no rolling angle and (B) an arbitrary rolling angle [11].

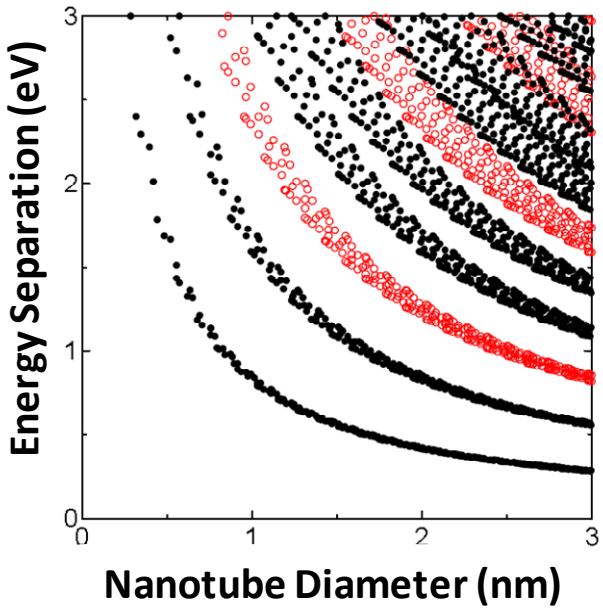

Figure 1.9: Kataura plots showing the diameter dependence on the energy separation for the bands and subbands of carbon nanotubes. The black dots represent semiconducting nanotubes while the red ones represent metallic nanotubes [12].

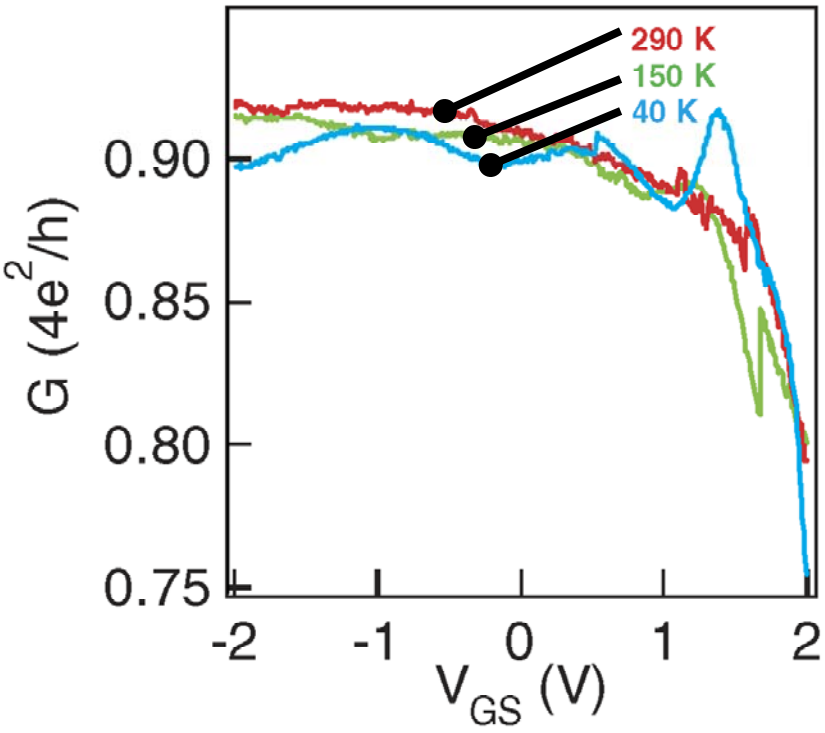

Figure 1.10: Conductance as a function of gate bias for various temperatures for a near ballistic metallic nanotube [13].

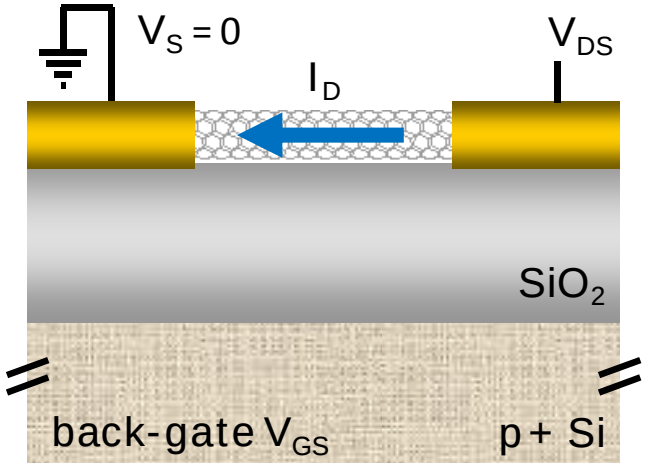

Figure 1.11: Cross section of a typical back gated CNTFET [17] used in this study.

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CHAPTER 2
EXPERIMENTAL PROCEDURES

2.1 Device Fabrication

As mentioned in the previous chapter, the devices used in this study are bottom-gated CNTFETs. The device is an inverted MOSFET with the gate being on the bottom and the channel lying in the nanotube, which sits on top of a substrate and dielectric. Fabricating CNTFETs can be split into two processes, one that involves traditional semiconductor fabrication techniques and CNT growth itself, both of which will be discussed in great detail below.

2.1.1 Carbon Nanotube Growth

In the beginning CNTs were grown using an arc discharge method meant for producing fullerenes [1]. In this process an arc is created by running high currents between two graphite electrodes. The resulting soot would contain CNTs. The problem with arc discharge was that it produced nanotubes that were not pure and it randomly produced both SWNTs and MWNTs. To combat this problem a laser ablation process was developed by Richard Smalley's group at Rice [2]. This growth technique involves pulsing a laser at a target that is a mix of metal catalysts and graphite at very high temperatures (>1000 ^{o}C) under inert gas flow (Ar) in a small tube (~25 mm diameter). While this solved the purity problem and produced primarily SWNTs, laser ablation is not compatible with current semiconductor fabrication processes because the nanotubes are not grown on a semiconducting substrate. After laser ablation, nanotubes need to be transferred to a substrate. This is usually done by mixing the nanotubes into solution and then dropping it onto the desired substrate. Such transfer methods are very damaging to the CNTs as they mechanically introduce defects, as any chemical process will do.

To date the growth process that has shown the most promise for large scale production is the chemical vapor deposition (CVD) growth method. CVD is a standard method of growing epitaxial material layers that has long been used by the semiconductor industry. The way CVD works is by using gases that contain the elements of the desired material and flowing them into a heated chamber where the species will react to form the desired material and deposit on top of a substrate. In 1993, CVD was adapted to grow CNTs [3]. The advantage of CVD over previous growth methods was that it allowed nanotubes to be grown directly onto a substrate. In addition, through patterning of catalysts, at least the starting point of where nanotubes grew could be controlled [4]. Additional advances have also been made in CVD growth allowing for vertically aligned nanotube growth [5], centimeter long nanotubes [6], and aligned nanotube arrays [7]. In this study all nanotubes were grown via the CVD method. Nanotubes are grown in CVD by flowing a carbon feedstock gas into a chamber and reacting it with hydrogen at high temperatures. In the presence of a nano-size catalyst particle, a CNT will grow from the nanoparticle. The CVD chamber used in this study is pictured in Figure 2.1.

Using CVD to grow CNTs, there are five adjustable parameters: pressure, temperature, catalyst type/thickness, gas flow, and growth time. As the pressure of the chamber is lowered, so is the density of nanotubes grown. The gain is that the density becomes more consistent. In this study nanotubes were grown at 760 Torr. Changing the temperature will roughly change the diameter distribution of CNTs because it will change the size of the nanoparticles that roughly control the diameter of the nanotube. Therefore, a higher temperature will generally produce smaller diameter nanotubes. Caution must be taken if the temperature is lowered too much since the quality of CNTs grown gets worse

if the temperature is too low. Nanotubes in this study were grown at 900 ^{o}C. Different catalysts will grow with varying densities. Catalysts can either be evaporated metal or spun on nanoparticles in solution. In this study 2 Å of electron beam evaporated Fe was used as the catalysts. In reality the catalyst layer thickness is more than 2 Å; this is just the reading on the crystal monitor. To create nanoparticles from evaporated metals, the sample is held at high temperature (900 ^{o}C) for at least 30 min under a flow of Ar. The high temperature causes nano-sized beads to form from the evaporated metal. Evaporating thicker metal layers (~5 Å) will cause the beads to increase in diameter, leading to thicker diameter tubes. If an even thicker layer of metal is deposited, then it is even possible to grow vertically aligned nanotubes.

Gas flow rates have the biggest effect upon growth. The CVD reactor used in this study is equipped with four gasses: argon, hydrogen, methane (CH_4), and ethylene (C_2H_4). Each is controlled by a mass flow controller of a different flow range. Typically Ar is used for heating up and cooling the sample as it creates an inert environment and prevents anything inside the chamber from oxidizing. The two carbon feedstock gases are methane and ethylene. Both gases require the presence of hydrogen to help dissociate carbon from hydrogen. Hydrogen can also be used to dilute the ratio of hydrogen to carbon atoms in the chamber if its flow rate is increased enough. Typical flow rates for hydrogen in this study were in the range of 300–500 standard cubic centimeter per minute (SCCM). Methane by itself requires a high flow rate in order to generate high densities. The diameter distribution of methane growth also tends to be smaller. Ethylene by itself grows with very high densities as it has twice the carbon atoms of methane and dissociates from hydrogen at lower temperatures. Too much ethylene will result in carbon

soot being deposited instead of nanotubes. In this study a mix of methane and hydrogen was used. Typical methane flow rates were in the range of 500–700 SCCM and typical ethylene flow rates were in the range of 12–16 SCCM. The length of nanotubes depends on both the flow rate of gases during growth and the growth time itself. In this study nanotubes were grown from 15–20 minutes. Lowering the gas flow rates lengthens the tube but usually decreases nanotube density. Increasing the growth time will usually increase the length of nanotubes grown. However, if the gas flow rate is too high then it will not change the length of nanotubes grown by much. Also, if the growth time is too long, then some tubes will be burned up and the nanotube density will drop. All of these adjustable parameters are yet another reason why CVD is highly regarded, because it gives users the ability to engineer the results they want.

2.1.2 Turning CNTs into CNTFETs

Fabricating CNTFETs uses the same technologies as semiconductor fabrication. The only difference is that once nanotubes are grown or deposited onto a substrate, care must be taken to apply as little mechanical force to the sample as possible. Mechanical agitations such as sonication and simply blow-drying a sample too hard can introduce defects into nanotubes and even remove nanotubes from the substrate in some cases.

The first step in creating a back gated CNTFET is to deposit the gate dielectric. This is done by oxidizing a silicon wafer. The thickness used was 70–100 nm of dry thermal oxide. Dry oxide is preferred to steam or wet oxidation as dry oxide gives better oxide quality. The thinner the oxide can be made, the better, because if it is too thick it will trap injected charge. Such injected charge has been shown to contribute to hysteresis when measuring drain current versus gate voltage [8].

The next step depends on the catalyst used; if the catalyst is thick and can be seen under an optical microscope then they can be used as alignment marks. If the catalysts are not visible, then alignment marks must be put into the substrate. In this study, since only 2 Å of Fe was evaporated as the catalyst, alignment marks were patterned in via photolithography. After defining the alignment marks with a photoresist mask, a Freon (CHF_3) plasma etch was done to etch the uncovered SiO_2. The back side of the wafer was also etched to make sure good back gate contact could be made. Finally a dip into 1:10 buffered HF was done to make sure all the necessary oxide was removed. This allowed for the alignment marks to also be top side access to the back gate.

The next step is to deposit catalysts on top of the oxide. As mentioned before, the strength of CVD is that it allows control over the point from which the nanotube grows. To take advantage of this, we pattern another photoresist mask and photo-lithographically define the areas where we want to deposit Fe. In this case 3×3 μm squares were opened up. Following photolithography, 2 Å of Fe were evaporated with an electron beam evaporator. Finally, the substrate is placed into acetone to perform liftoff. The sample is now ready for CNT growth.

After growing CNTs, the last step is to deposit source and drain contacts to the nanotube. Since a thicker layer of metal must be deposited for the contacts than for the catalysts, a sacrificial resist layer (PMGI SF5 from Microchem) may be spun on before the photoresist is spun onto the substrate. The same sacrificial resist may be used with catalyst liftoff and in fact is cleaner than just using photoresist alone. Again the area where metal is to be deposited is defined with photolithography. The metal of choice to contact the nanotube is palladium (Pd). It has been shown in previous studies that

palladium makes ohmic contacts to nanotubes because of its high work function and also sticks to the nanotube better than other high work function metals such as gold [9, 10]. The drawback of Pd is that it does not stick to SiO_2. For sticking purposes a Ti layer may be patterned and placed down before the Pd. However, the Ti cannot touch the nanotube as it forms a Schottky contact.

An SEM of the finished device is shown in Figure 2.2. The electrodes have a channel that is semicircular with one "finger" extending over the catalyst to contact one end of the nanotube. The reason for the semicircular electrode is to have an approximate estimation of nanotube length. Of course, the nanotube may not grow straight across and would hence be longer than the electrode separation. In cases where a large and statistically meaningful amount of data is taken, it is helpful to know the approximate length of the nanotube being measured to check trends associated with nanotube length.

2.2 Measurements and Characterization

After CNTFETs have been made, they need to be characterized and measured. Since the current masks puts down 1600 pairs of electrodes, the first thing that is needed is to map out which devices are actually connected by nanotubes. After quickly mapping out the connections, careful measurements can be made on the CNTFETs. If additional dimensional data is needed, it can be found through more careful characterization methods.

2.2.1 Characterizing Carbon Nanotubes

Using what is known about CNTs from the previous chapter, each device can be placed into certain categories with simple and quick electrical measurements. Using two electrical probes and a substrate chuck that may be electrically biased, the CNTFET's

drain, source, and gate can be connected. The first test done is a drain current I_D vs. gate voltage V_{GS} measurement. Here V_{GS} is swept while at the same time the drain voltage V_{DS} is biased at low voltage and I_D is monitored. If the device is connected by semiconducting tubes only, then a sharp subthreshold slope will be observed as the device turns on and off. If the device is connected by a metallic tube, then its I_D will vary little with the gate bias. In Figure 2.3 a typical I_D vs. V_{GS} plot is shown for both a semiconducting and metallic nanotube. From this measurement it can be quickly determined which devices are connected and contain either semiconducting or metallic nanotubes.

The next measurement while mapping out devices is an I_D vs. V_{DS} scan, often referred to as the *I-V* scan. In this measurement the drain voltage is swept over a range of voltages while the gate voltage is biased at a constant voltage and the drain current is monitored. For semiconducting nanotubes, the gate voltage will dictate the population of carriers in the nanotube, thus varying the current. In metallic tubes the gate voltage will have a very minimal effect. For mapping purposes the gate voltage was biased at $V_{GS} \geq$ -15 V, ensuring that all connected devices would be turned on. Since the study was focused primarily upon single connected SWNTs and not MWNTs or multiply connected devices. It was important to look at the saturation current. Nanotubes that saturated at $I_D \leq 25$ μA were considered to fall under that category. Figure 2.4 gives an example of what that plot will look like. If devices saturated above the 25 μA limit, they would be considered to have multiple connections or to be connected by MWNTs. If that was the case, increasing V_{DS} would eventually cause nanotubes to break through Joule heating until just one nanotube remained, as seen in Figure 2.4. The next feature to look at is the low bias ($V_{DS} < 1$ V) portion of the curve. By taking the inverse slope at low bias, a rough

estimate of the contact resistance can be determined. Good ohmic contacts had contact resistances of $R_C \sim 30–50$ kΩ.

Sometimes, it is necessary to know the exact diameter of the nanotube. Knowing the nanotube diameter can help determine if the CNT is a SWNT or MWNT. Typical SWNT diameters have been reported in the range of 0.5–4 nm. To measure the diameter of individual nanotubes, an atomic force microscope (AFM) was used in tapping mode. An example of an AFM image of a nanotube is given in Figure 2.5. While AFM normally gives a very accurate measurement of height displacement of a surface, its accuracy is limited for measuring nanotube diameter. First, the nanotube is often "squashed" because strong van der Waals interactions from the substrate pull the nanotube to the surface. Second, there are surface interactions between the tip and the nanotube. In the case of graphene, the AFM tip is attracted to the graphene surface and makes the graphene sheet appear thicker than it really is. Because of these uncertainties, we estimate the error in diameter introduced by AFM to be about ±0.4 nm. AFM also gives the length of the nanotube, although that can also be measured via SEM.

2.2.2 Measuring Impact Ionization in CNTFETs

In order to probe II, several different measurements were conducted. Mostly, they are variations on I_D vs. V_{GS} and *I-V* measurements discussed in the previous section. The condition needed to induce II is that there must be a high field present. This means that devices need to be measured at high bias. Doing such measurements in air is dangerous as the breakdown mechanism in air is thought to be oxidation, which happens around 600 ^{o}C, a temperature easily obtainable through Joule heating [11]. To prevent a quick breakdown and to allow development of an avalanche induced current upkick,

measurements are made under vacuum in a vacuum probe station. Figure 2.6 compares nanotubes of similar lengths, showing how vacuum can protect nanotubes from breaking. In addition, the vacuum probe station allows for samples to be studied in cryogenic temperatures. Another advantage of doing measurements in vacuum is that hysteresis in the I_D vs. V_{GS} sweep is minimized as water molecules (which dope the nanotube p-type in air) are desorbed from the surface [12]. However, while water molecules are desorbed from the carbon nanotube surface, H_2 is also desorbed from the Pd contacts. The desorbing of water will cause the work function of Pd to decrease and the contacts to worsen. If devices are left in vacuum long enough they will become ambipolar and eventually n-type as the work function of the Pd continues to decrease. To prevent this from impacting the data, measurements were taken within an 8 h of sample loading.

2.3 Figures

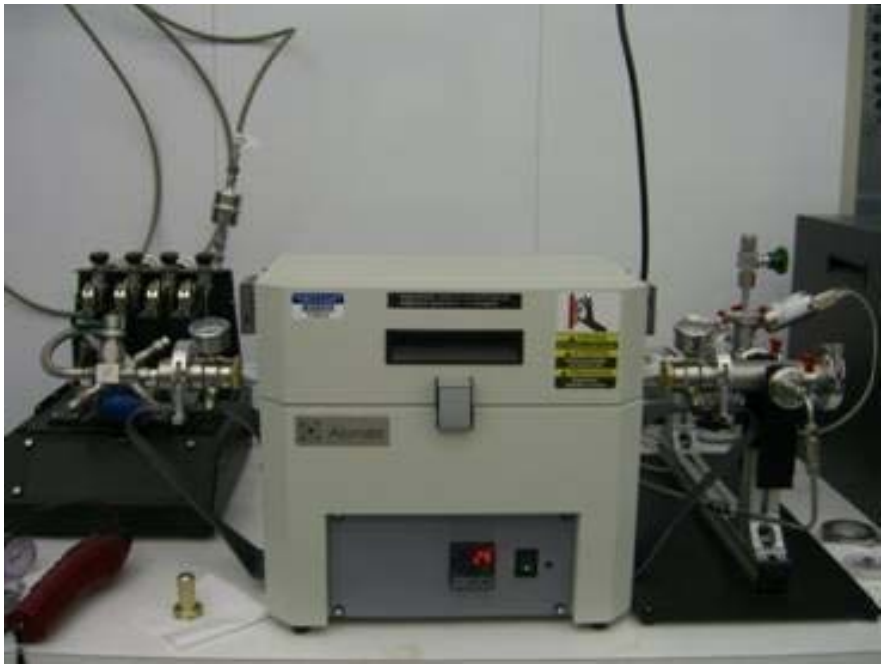

Figure 2.1: Photograph of the Atomate® carbon nanotube chemical vapor deposition reactor used in this study.

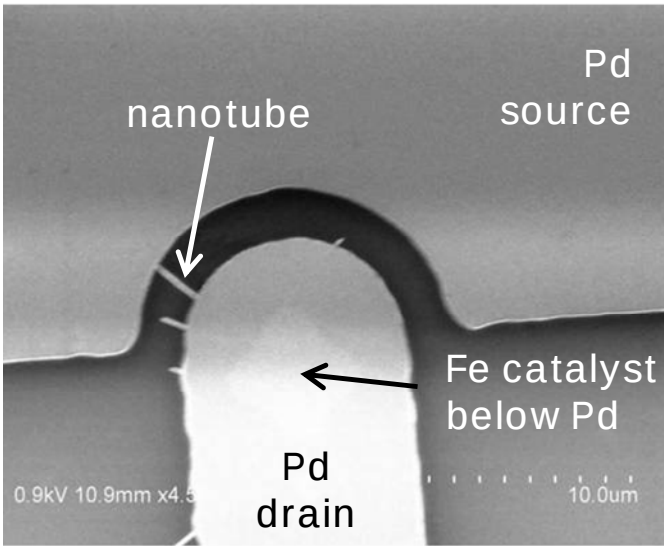

Figure 2.2: Scanning electron microscope (SEM) top-view image of a fabricated device. Semicircular electrodes are used for tighter control of device length. Scale bar is 10 μm [13].

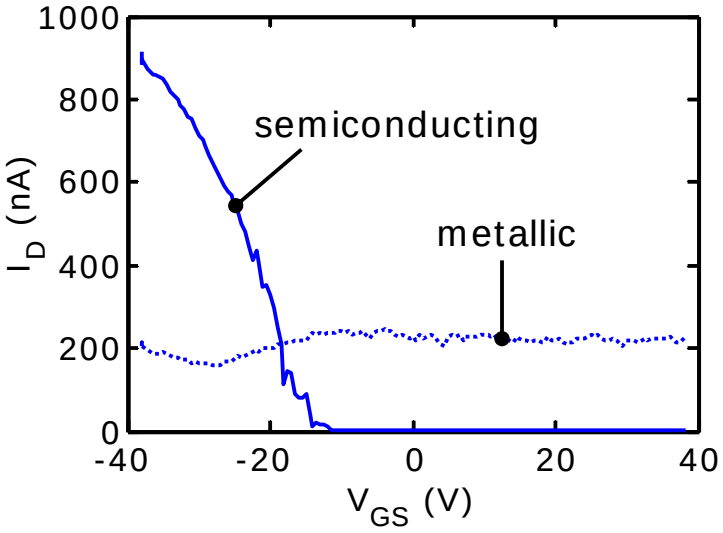

Figure 2.3: Back-gate voltage dependence (V_{GS}) of semiconducting and metallic SWNT showing typical on/off ratios [13].

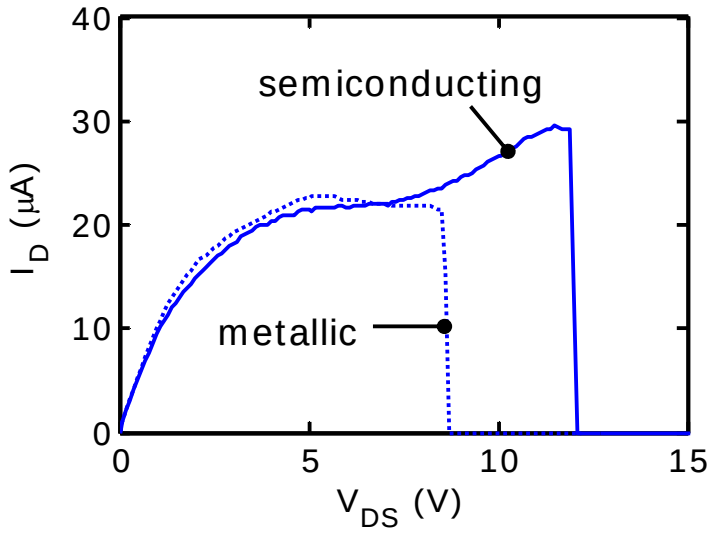

Figure 2.4: Drain voltage (V_{DS}) dependence up to breakdown in air of semiconducting and metallic SWNTs. Metallic device saturates before breakdown, whereas semiconducting tube displays an up-kick in current. Compared devices have similar diameter $d \sim 2.5$ nm and length $L \sim 0.8$-1.1 μm [13].

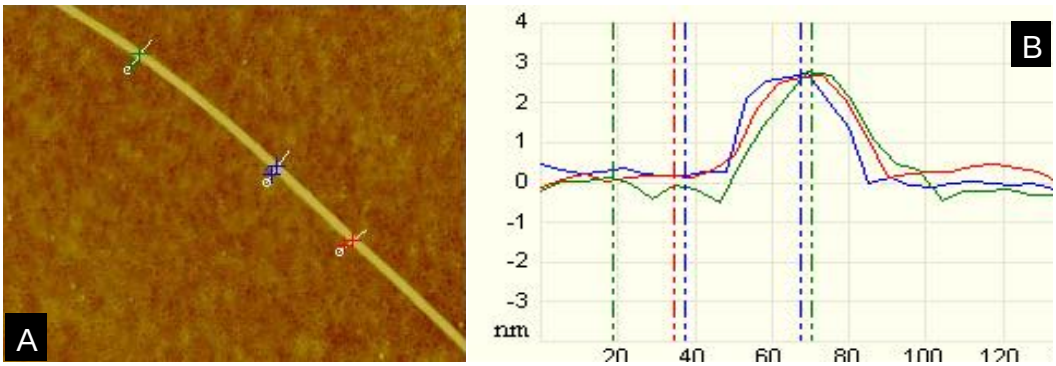

Figure 2.5: (A) Typical atomic force microscope (AFM) height profile of a single-walled carbon nanotube with its (B) cross-sectional height given .

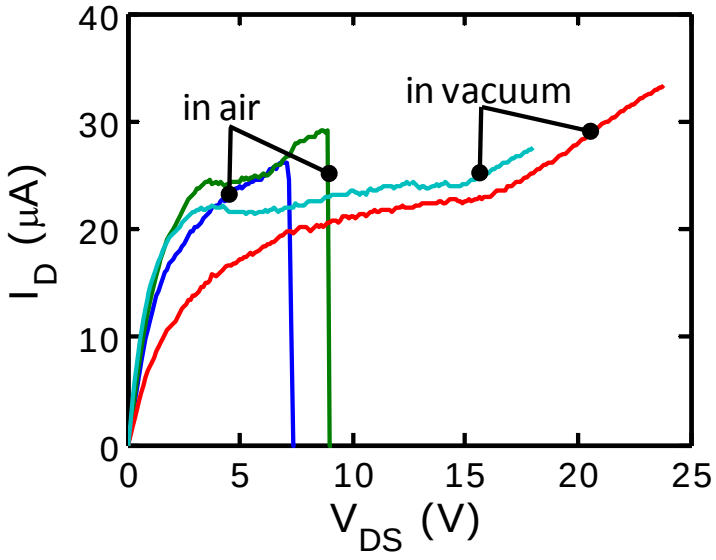

Figure 2.6: Two "typical" air breakdowns vs. two vacuum sweeps safely going to much higher voltage, for nanotube devices of comparable length, ~2.5 μm.

2.4 References

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CHAPTER 3
AVALANCHE-INDUCED CURRENT ENHANCEMENT IN SEMICONDUCTING CARBON NANOTUBES

3.1 Current Enhancement in Carbon Nanotubes

While quasi-ballistic transport at submicron lengths [2] and low-field mobility in longer, diffusive samples [3] has been studied in great detail in carbon nanotubes, much is still unknown about diffusive transport at high fields (>1 V/μm). This regime sets the peak current-carrying ability, and provides a glimpse into the behavior under extreme electrical stress conditions. For instance, the maximum current of long *metallic* single-wall nanotubes (m-SWNTs) is 20–25 μA when limited by Joule heating and optical phonon scattering [4, 5], which appears to be exceeded only in submicron, quasi-ballistic samples [2]. The maximum current capacity of long *semiconducting* single-wall nanotubes (s-SWNTs) under diffusive transport is less established, although a 25 μA limit has been suggested for single-band conduction [6]. However, experimental data indicates this limit is exceeded under ambipolar transport [7], and theoretical estimates suggest this value can be surpassed when multiple subbands are involved [8].

Current vs. drain-source voltage (V_{DS}) measurements were made in air and vacuum. In air, metallic nanotubes saturate from self-heating and strong electron-phonon scattering [4] up to Joule breakdown, as previously discussed in Chapter 2. By contrast, most semiconducting tubes turned on at large $|V_{GS}|$ exhibit a sudden current increase before Joule breakdown. Additional measurements carried out in vacuum (~10^{-5} Torr) allow further study of the current up-kick without breaking the nanotubes by oxidation. It is important to note that devices were measured in the reverse bias regime, with

This chapter is taken from [1].

$V_{GS} < 0 < V_{DS}$ and $|V_{GS}| > |V_{DS}|$ [8]. By contrast, in Schottky mid-gap contacted devices, the ambipolar regime $V_{DS} < V_{GS} < 0$ "splits" the potential drop along the nanotube, resulting in lower longitudinal electric fields [7-9] and transport by both electrons and holes. In the reverse bias regime, holes are the majority carriers in our s-SWNTs until the avalanche mechanism partially turns on the conduction band (Figure 3.1).

At first glance, several mechanisms may be responsible for the current increase at very high fields in our s-SWNTs, all various forms of "soft" (reversible) breakdown [10]. These are Zener band-to-band (BB) tunneling, avalanche impact ionization (II), and thermal generation current. Under BB transport, electrons tunnel from the valence to the conduction band. The probability is evaluated as $P_{BB} \sim \exp(-E_G^2/q\hbar v_F F)$, where E_G is the band gap (~0.84/d eV/nm), v_F is the Fermi velocity, and F is the electric field [11]. During avalanche II, holes gain high energy in the valence band, then lose it by creating electron-hole pairs (EHPs) as shown in Figure 3.1. Inelastic optical phonon (OP) emission is the strongest process competing with II, given the large OP energy ($\hbar\omega_{OP}$ ~ 0.18 eV). The II probability is estimated as $P_{II} \sim \exp(-E_{TH}/q\lambda_{OP,ems}F)$ [12-14]. We take $\lambda_{OP,ems} \sim 14d$ nm as the spontaneous OP emission mean free path (MFP) by holes or electrons [14], and E_{TH} is the avalanche energy threshold. Comparing the two mechanisms in Figure 3.2 suggests impact ionization is considerably more likely for the electric field and nanotube diameter range in this study. BB transport becomes important as a result of sudden spatial changes in electrostatic or chemical doping, leading to local fields of the order 100 V/μm (1 MV/cm) or higher [15, 16]. Thermal generation is experimentally investigated, and is also found to make a negligible contribution, as explored in more detail below.

Not all semiconducting nanotubes exhibit current up-kick at high fields. Previous work by Marty et al. has shown no current up-kick at high bias, but has instead detected radiative exiton recombination [17], which is a competing mechanism with II. This was reasonably attributed to direct exciton annihilation, rather than the avalanche generation of free carriers. By contrast, our nanotubes have ~2x larger diameters, thus approximately half the band separations and exciton binding energies, and ohmic Pd contacts rather than Schottky Co contacts. In addition, all our measurements were made in vacuum, allowing repeated study of the current up-kick, which was not always observable in air before Joule breakdown. While excitonic generation and recombination may play a role in our samples, we suggest that the current increase is possible because most free EHPs are generated in the high-field region within a few mean free paths (10-100 nm) of the drain. Thus, generated electrons are swept out into the electrode by the high field within 0.1-1 ps (Figure 3.2), much faster than the recombination lifetimes (10-100 ps) [18]. In addition, the high temperatures and high fields in these conditions contribute significantly to exciton instability, despite their relatively high binding energy.

3.2 Impact Ionization in Carbon Nanotubes

Previous theoretical work has shown II in s-SWNTs is not possible until the third subband is occupied [14], due to angular momentum conservation as illustrated. Perebeinos et al. have calculated the II rate in a nanotube, and their result is illustrated in Figure 3.3, clearly showing that there is no II occurring in the first two subbands. The II threshold energy measured from the edge of the first band scales as $E_{TH} \sim 3/2E_G \sim 1.26/d$ (nm), which is greater than the band gap, as is typical in other semiconductors [19, 20]. To determine if the third subband is populated in our experiments, we look at the

nanotube density of states (DOS) in Figure 3.4. Each Van Hove singularity represents the beginning of a subband. As V_{GS} is lowered beyond threshold, the Fermi level inside the nanotube shifts to the right on the DOS plot and the third subband begins to fill at approximately $|V_{GS}\text{-}V_T| \sim 15$ V. The observed V_T for our devices is in the range of -7 to -15 V. Thus, filling the third subband is within reach experimentally, as avalanche is seen at various V_{GS} and further discussed below. In addition, we find that direct injection into higher subbands at the contacts is also possible, as previously suggested [21]. We estimate this in Figure 3.5 using a WKB integral to calculate the conductance associated with direct injection into the first three subbands at the Pd electrode. Naturally, injection into higher subbands depends strongly on voltage, and while direct injection into the third band is possible, we expect that highfield intervalley scattering [22, 23] and gate-controlled charge distribution (Figure 3.4) are primarily responsible for populating the higher subbands.

3.2.1 Experimental Testing

The effects of gate voltage, nanotube length, and temperature on the avalanche current are shown in Figure 3.6. First, for a given length, a similar current up-kick is observed at high lateral fields at any gate voltage V_{GS} beyond threshold. That is, the four data curves converge on the "up-kick" region at high lateral drain voltage V_{DS} in Figures 3.6A and 3.6B. Second, for a similar diameter (similar band separations and II threshold E_{TH}), the onset of the avalanche up-kick is seen around the same approximate *field* ($\sim V_{DS}/L$), not the same drain voltage. The two data sets in Figures 3.6A and 3.6B suggest that filling the third subband at large gate voltage is a necessary, but not sufficient condition to induce current enhancement through hole avalanche. A high lateral electric

field set by the drain voltage is also required to create the signature up-kick in the measured *I-V* characteristics.

An important feature of the avalanche process in many semiconductors such as silicon is the negative temperature dependence of the II coefficient [24]. As the phonon scattering rate increases with temperature, free carriers gain less energy from the field and the II rate decreases at higher temperatures. Here, such trends are examined in Figure 3.7, showing experimental data taken from 150 K to 300 K. Unlike in silicon, we observe negligible temperature dependence of the high-bias impact ionization region. The essential difference lies in that the optical phonon (OP) emission MFP ($\lambda_{OP,ems}$) varies minimally with temperature in SWNTs. As the OP energy is much greater than in other materials, the OP occupation $N_{OP} = 1/[\exp(\hbar\omega_{OP}/k_B T)-1]$ is very small, $\ll 1$, where k_B is the Boltzmann constant. Following [4], the spontaneous OP emission MFP can be written as $\lambda_{OP,ems} = [N_{OP}(300)+1] / [N_{OP}(T)+1]\lambda_{OP,300}$ where $\lambda_{OP,300} \approx 14d$ [14]. This MFP is shown for two diameters in Figure 3.8, illustrating the negligible temperature variation. The lack of temperature dependence and that of a significant current (Joule heating) dependence of the up-kick also indicates there is no significant contribution from thermal current generation. Quite the opposite, given the generation of EHPs rather than OPs during II, a lowered Joule heating rate in the highest field region near the drain is expected.

3.2.2 Modeling Avalanche Current in CNTFETs

In order to better understand the field dependence of the avalanche process, an existing SWNT model [4] has been modified by including II as an additional current path through a parallel resistor. The choice is motivated by the physical picture in Figure 3.1,

which shows electron transport in the conduction band "turning on" as an additional channel at fields high enough to induce hole-driven II. The expression for this resistor is given as $R_{II} = R\exp(E_{TH}/q\lambda_{OP,ems}F)$, where R is for single-band transport, computed self-consistently with the SWNT temperature [4]. The results are shown in Figure 3.9 with $\lambda_{OP,ems}$ included as mentioned above, and without any other adjustable parameters. Despite being an "augmented" single-band model, the simulation correctly captures the experimentally observed current up-kick and its delayed voltage onset. The simple analysis also allows us to gain physical insight into the avalanche process, and to intuitively extract a few more key parameters. More steps in the future, such as inserting multiple sub-bands, will be taken to more accurately model the current up-kick.

3.2.3 A Novel Method of Extracting Inelastic Optical Phonon Emission Length

In the parallel resistor approach, the resulting avalanche current is derived to be $I_{II} \approx I_S\exp(-E_{TH}/q\lambda_{OP,ems}F)$, where I_S is the saturation current reached before II becomes significant. Inserting the expected diameter dependence $E_{TH} \approx E_1/d$ and $\lambda_{OP,ems} \approx \lambda_1 d$, we obtain $I_{II} \approx I_S\exp(-E_1/q\lambda_1 F d^2)$, where E_1 and λ_1 are the threshold energy and MFP for a nanotube of diameter 1 nm. Consequently, the average field at which $I_{II} = I_S/2$ is given by $\langle F_{TH}\rangle \approx E_1/q\lambda_1 d^2\ln(2)$. The experimental data in Figure 3.10A is used to extract this field (but not the peak field) in our devices by extrapolating from the tail region to $\langle F_{TH}\rangle$ at which the current reaches one half the saturation values. These values are plotted against $1/d^2$ for nanotubes of several diameters ($d \sim$ 2.2-3.6 nm) in Figure 3.10B. The slope of the linear fit thus scales as the ratio between the II threshold energy and the inelastic MFP, E_1/λ_1. However, the avalanche process is a strong function of the field, and most EHPs are generated at the peak field, $F_{TH,MAX}$. The latter is estimated by noting that the

potential near the drain has a dependence $V(x) \approx \ell F_0 \sinh(x/\ell)$, where $F_0 \sim 1$ V/μm is the saturation velocity field [6] and ℓ is an electrostatic length scale comparable to t_{ox} [9, 25, 26]. Fitting this expression to our voltage conditions and nanotube dimensions, we find $F_{TH,MAX}/\langle F_{TH} \rangle \approx 4.5$ for the $L = 1$ μm device, and 3.5 for $L = 2$ μm. Thus, using the peak instead of the average field, the empirically extracted slope gives $E_1/\lambda_1 \sim 0.088$ eV·nm, where we take $E_1 = 1.26$ eV as the bottom of the third subband. Accounting for fit errors, this yields $\lambda_1 = 15 \pm 3$ nm as the inelastic OP emission MFP for $d = 1$ nm, or generally $\lambda_{OP,ems} = \lambda_1 d$. This value is in good agreement with the theoretically predicted $14d$ nm in [14], and our approach demonstrates a novel empirical method for extracting this important transport parameter from high-field electrical measurements.

3.3 Figures

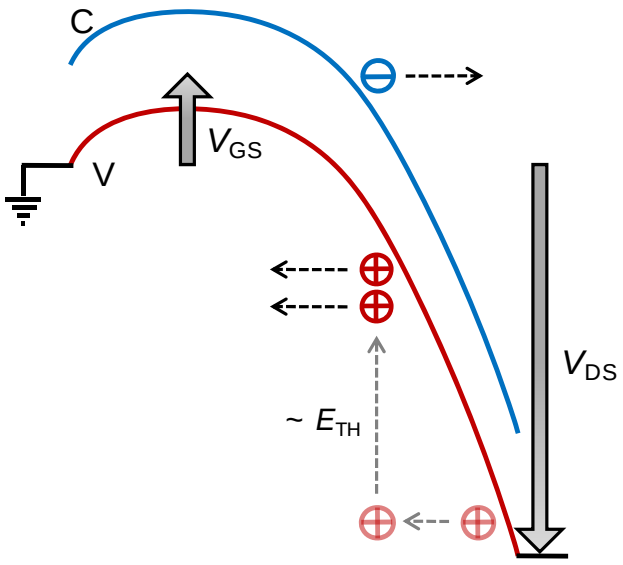

Figure 3.1: Schematic band diagram of a carbon nanotube of EHP generation under reverse bias conditions [1].

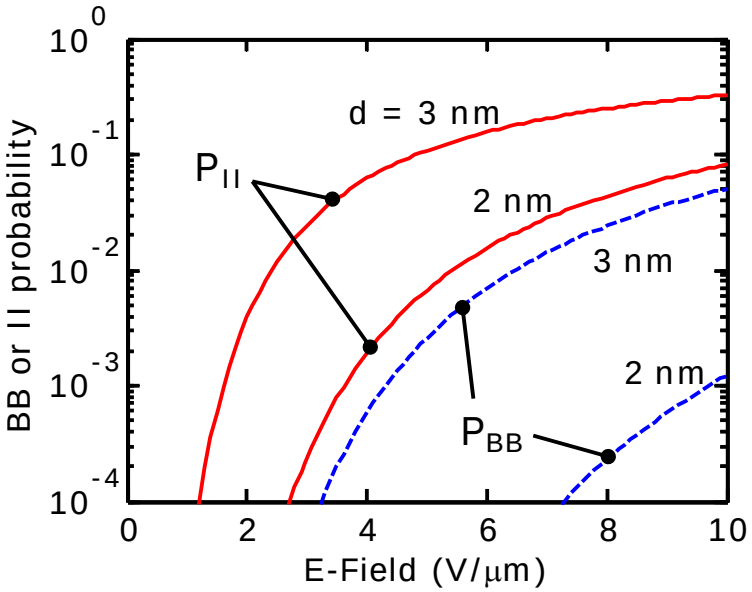

Figure 3.2: Probability of impact ionization (II) and Zener band-to-band tunneling (BB) vs. electric field along the nanotube, for the diameters and field range of interest [1].

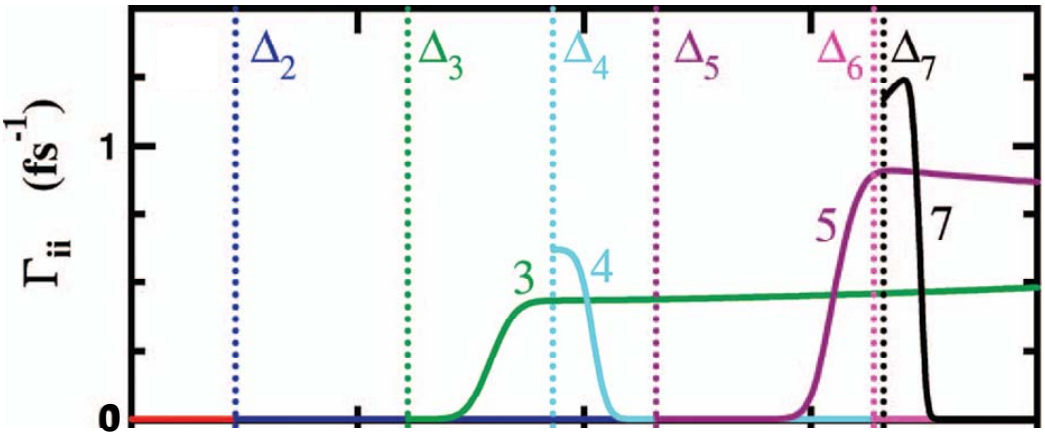

Figure 3.3: Impact ionization for a (25,0) carbon nanotube. Each dotted line represents a subsequent subband. No impact ionization is observed in the first two subbands [14].

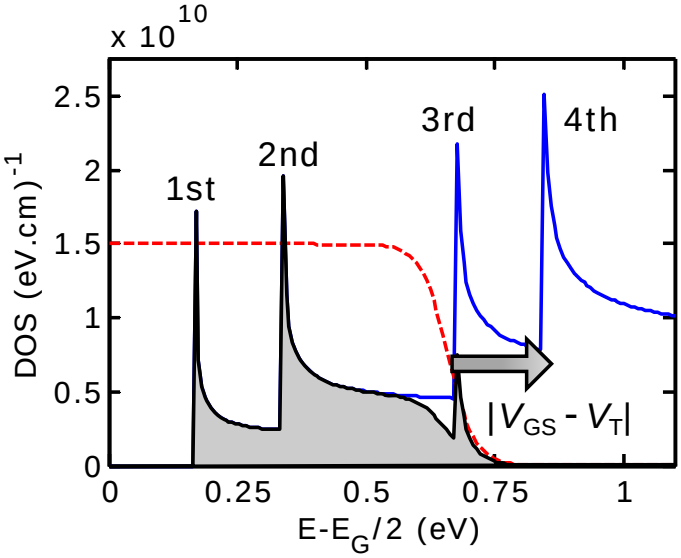

Figure 3.4: Computed density of states (DOS) showing the first four subbands. The second band begins to fill at $|V_{GS}-V_T| \sim 5$ V and the third at $|V_{GS}-V_T| \sim 15$ V, as pictured [1].

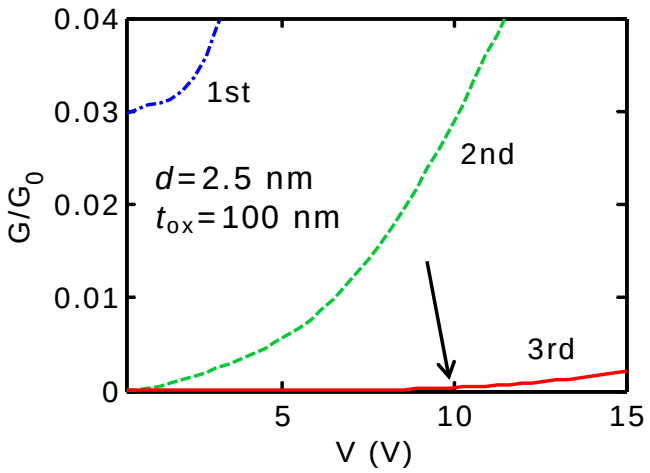

Figure 3.5: Contact conductance of the first three subbands under direct injection from the Pd electrode. The arrow indicates approximate voltage at which direct injection into the third subband becomes significant [1].

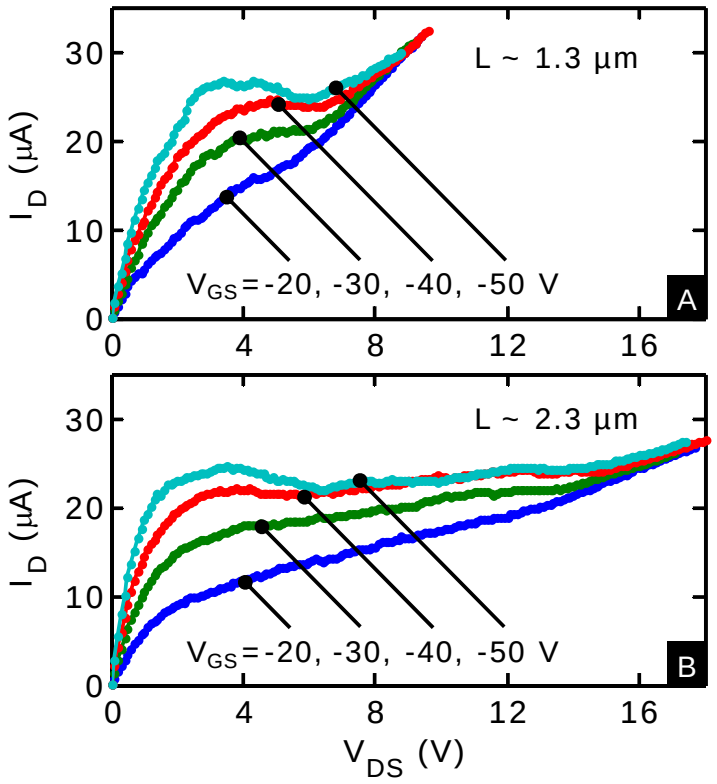

Figure 3.6: Length dependence of impact ionization tail. Measured reverse bias current vs. drain voltage (V_{DS}) in vacuum with applied back-gate V_{GS} for two s-SWNTs with similar diameter (d ~ 2.5 nm) but with device lengths of (A) L ~ 1.3 μm and (B) L ~ 2.3 μm. The onset voltage for the avalanche "up-kick" scales as the lateral *field* and appears independent of V_{GS} [1].

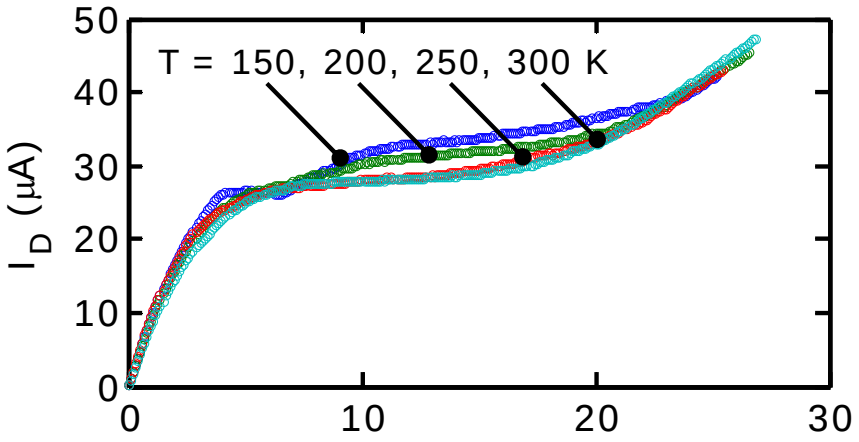

Figure 3.7: Temperature insensitivity of impact ionization tail. Measured reverse bias I_D-V_{DS} curves for a s-SWNT with $d \sim 2.2$ nm and $L \sim 2.2$ μm, in vacuum [1].

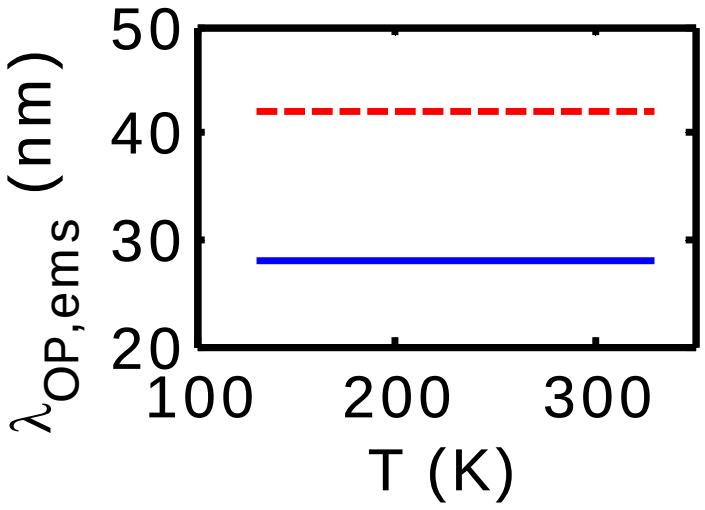

Figure 3.8: Optical phonon emission mean free path in nanotubes ($\lambda_{OP,ems}$) calculated for two diameters vs. temperature. Unlike other materials, $\lambda_{OP,ems}$ does not vary a lot with temperature [1].

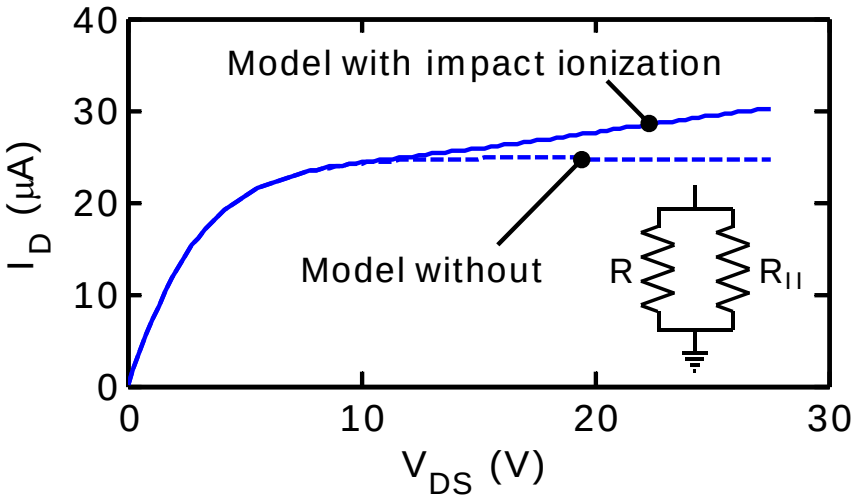

Figure 3.9: Model including and excluding impact ionization as a second parallel channel which begins to open up at high field [1].

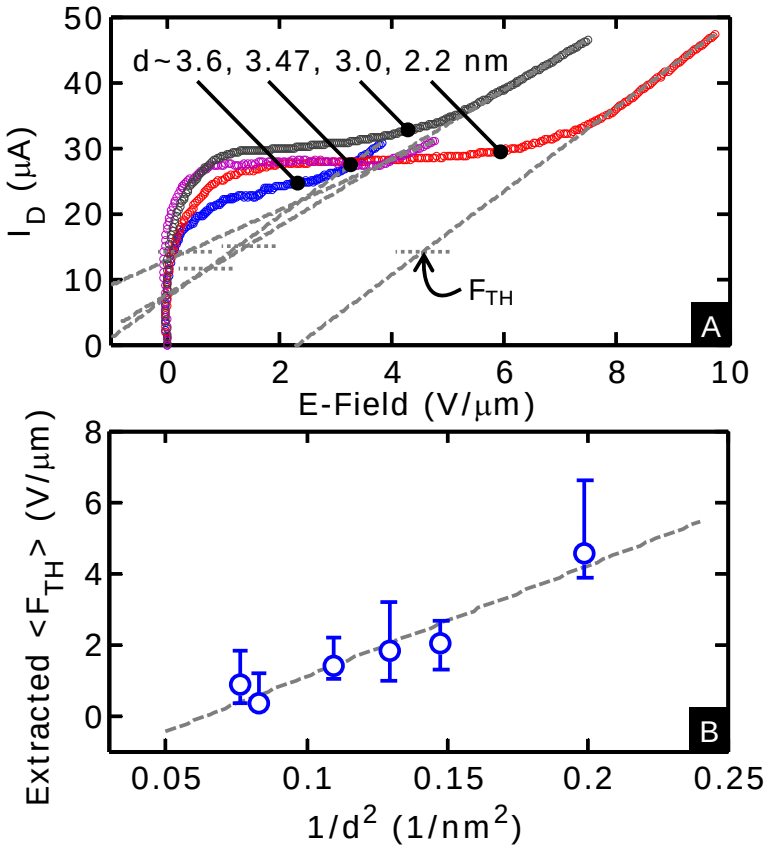

Figure 3.10: Diameter dependence of avalanche threshold field F_{TH}. (A) Current vs. average channel field $(V_{DS}\text{-}I_D R_C)/L$ for several s-SWNT diameters. (B) Extracted average $\langle F_{TH} \rangle$ vs. $1/d^2$. The uncertainty in diameter from AFM measurements is 0.4 nm [1].

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CHAPTER 4
CONCLUSION

4.1 Carbon Nanotube I-MOS

As mentioned in the introduction, the problem with the I-MOS is its operating voltage. Attempts to lower the operating voltage have included investigating different materials and applying new technologies such as nanowires [1]. Ideally, the I-MOS needs a material with a band gap that is small so that the breakdown field is low, but not so small that BB comes into play. Indeed SWNTs satisfy this requirement. When compared to Si and Ge in Table 4.1, SWNTs have ~5x lower breakdown field [2-4]. One other benefit that would come out of using nanotubes is that since the electron and hole effective masses are the same, so are their II rates [2], thus making it easier to design circuits in a CMOS fashion. Finally, nanotubes have higher mobility than typical semiconductors like Si, Ge, or GaAs, and quasi-ballistic behavior at room temperature in relatively long (~0.5 μm) samples [5].

Still, there are several unknowns that will be worth studying in order to maximize the design for a CNT-based I-MOS. It is still unknown how top-gated CNTFETs will affect II. Since the electric field is thought to be nonuniform across the length of the nanotube, the placement of the top-gate will be very important. To lower the turn-on voltage below 1 V it will be necessary to find out what configuration enhances the lateral field, as that is what controls the onset of II [3]. It may also be fruitful to study possible light emission from excitons [2, 6] as this is a competing mechanism for II. Minimizing light emission may further increase the II current and thus lower subthreshold slope. Finally, the reliability of nanotubes under avalanche current must be studied. While preventing direct exposure to air will prevent breakdown as caused by oxidation, it is still

unknown how stable nanotubes will be at such high bias. The main concern here is heat dissipation for nanotubes wrapped in a dielectric, as the latter have low thermal conductivity. Understanding heat dissipation and thermal boundary resistance between the dielectric and nanotube will also prove to be very important.

4.2 Summary

In summary, a remarkable current increase beyond 25 μA is observed in semiconducting SWNTs driven into avalanche impact ionization at high fields (~10 V/μm). By analyzing near-breakdown *I-V* data, the avalanche process is found to be nearly temperature independent, but strongly diameter dependent ~exp(-1/d^2), unlike in other materials. In addition, a novel estimate of the inelastic optical phonon scattering length $\lambda_{OP,ems} \approx 15d$ nm is obtained by fitting against a model of the high-field current "tail." It is noted that upper sub-band transport must be considered at high bias, and has a significant effect on the current carrying capacity of such nanomaterials. The results also suggest that avalanche-driven devices with highly non-linear characteristics can be fashioned from semiconducting carbon nanotubes, such as a CNT based I-MOS.

4.3 Table

Table 4.1: Impact Ionization parameters comparing SWNTs to Ge and Si [2-4]

Material	Band Gap E_G (eV)	Avalanche Field (V/μm)	Electron II Rate (1/s)		Hole II Rate (1/s)
SWNT	~0.3	~5	$5x10^{14}$	=	$5x10^{14}$
Ge	0.66	~20	$4x10^{12}$	<	$6x10^{12}$
Si	1.1	~30	10^{12}	>	$3.5x10^{11}$

4.4 References

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APPENDIX A
PROCEDURES FOR MAKING CNTFETS ON SILICON

A.1 Oxidation

1. Degrease wafer with acetone, methanol, and isopropyl alchohol (IPA).
2. Perform buffered oxide etch (BOE) with hydrofluoric (HF) to etch away native oxide.
3. Piranha etch (H_2SO_4 and H_2O_2) for 15 min followed by 20 min rinse in de-ionized (DI) water.
4. Oxidize wafer in thermal oxidation chamber at 1150 ^oC under 5 psi of dry oxygen flow.
5. Characterize oxide thickness using ellipsometry.

Note: The time between steps 2 and 3 should not exceed 1 h; otherwise, a native oxide will grow.

A.2 Etch

1. Degrease wafer with acetone, methanol, and isopropyl alchohol.
2. Bakeoff at 125 ^oC for at least 120 s.
3. Spin on hexamethyldisilazane (HMDS) and then photoresist (PR) S1813 from Rohm and Haas at around 3000 rpm for 30 s.
4. Prebake at 110 ^oC for 75-90 s.
5. Expose wafer with a contact aligner using a dosage of 50–75 mJ.
6. Develop off PR with MF-319 from Rohm and Haas.
7. Postbake at 110 ^oC for 120-135 s.
5. Use CHF_3 in the plasma freon reactive ion etcher (RIE) to etch.
6. Etch down to Si with a BOE etch.
7. Remove PR in acetone.

A.3 Depositing Catalysts

1. Piranha etch for at least 10 min. An alternative is to do an O_2 plasma scum in an RIE.
2. Bakeoff at 200 ^oC for at least 120 s.
3. Spin on Polymethylglutarimide (PMGI) SF6 from MICROCHEM at 5000 rpm for 30 s.
4. Postbake at 175 ^oC for 5 min exactly.
5. Spin on PR S1813 at 5500 rpm for 30 s.
6. Prebake at 110 ^oC for 75-90 s.
7. Expose wafer with a contact aligner using a dosage of 67.5 mJ.
8. Develop off PR with MF-319. Make sure you can see the substrate through the catalyst holes.
9. Postbake at110 ^oC for 120-135 s.
10. Deposit 2 Å of Fe using an electron beam evaporator.
11. Lift off in remover PG from MICROCHEM. When removing the sample from remover pg soak it in IPA for a bit and then degrease it.

A.4 Nanotube Growth

1. After inserting sample into Atomate carbon nanotube chemical vapor deposition chamber, flow all gases and leak check the system.

2. Heat up the furnace to 900 ^{o}C under argon flow.
3. Anneal sample under argon flow at 900 ^{o}C for at least 30 min.
4. Flow in carbon feedstock. See Chapter 2 for suggestions on flow settings.
5. Cool sample down under argon flow.

A.5 Depositing Metal Contacts

1. Bakeoff at 200 ^{o}C for at least 120 s.
2. Spin on PMGI SF6 at 4000 rpm for 30 s.
3. Postbake at 150 ^{o}C for 5 min exactly.
4. Spin on PR S1813 at 5500 RPM for 30 s.
5. Prebake at 110 ^{o}C for 75-90 s.
6. Expose sample with a contact aligner using a dosage of 15–40 mJ.
7. Develop off PR with MF-319.
8. Postbake at110 ^{o}C for 120-135 s.
9. Deposit metal using the CHA evaporator.
11. Lift off in remover PG. When removing the sample from remover PG, soak it in IPA for a bit and then degrease it.