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Improved gradual resistive switching range and 1000× on/off ratio in HfO_x RRAM achieved with a $Ge_2Sb_2Te_5$ thermal barrier

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ABSTRACT

Gradual switching between multiple resistance levels is desirable for analog in-memory computing using resistive random-access memory (RRAM). However, the filamentary switching of HfO_x-based conventional RRAM often yields only two stable memory states instead of gradual switching between multiple resistance states. Here, we demonstrate that a thermal barrier of $Ge_2Sb_2Te_5$ (GST) between HfO_x and the bottom electrode (TiN) enables wider and weaker filaments, by promoting heat spreading laterally inside the HfO_x. Scanning thermal microscopy suggests that HfO_x + GST devices have a wider heating region than control devices with only HfO_x, indicating the formation of a wider filament. Such wider filaments can have multiple stable conduction paths, resulting in a memory device with more gradual and linear switching. The thermally enhanced HfO_x + GST devices also have higher on/off ratio ($>10^3$) than control devices ($<10^2$) and a median set voltage lower by approximately 1 V (~35%), with a corresponding reduction of the switching power. Our HfO_x + GST RRAM shows 2× gradual switching range using fast (~ns) identical pulse trains with amplitude less than 2 V.

Abundant-data computing requires significant data movement to and from off-chip memory, resulting in a "memory-wall bottleneck," where speed and energy efficiency are dominated by the data movement.[1] In order to solve this memory-wall bottleneck, fine-grained access between memory and logic is required,[2] for which two types of solutions exist: (i) integrating multi-bit digital memory on-chip with high capacity and (ii) in-memory computing, a type of neuromorphic computing where some part of the computation is done inside the memory, reducing data movement between computing and memory.[3,4] In-memory computing requires storage of analog values, which requires resistive memories to switch gradually between different resistive states.

Among possible candidates for in-memory computing, resistive random-access memory (RRAM) is one of the emerging nonvolatile memory technologies that is highly scalable, back-end-of-line (BEOL) compatible, and capable of low-energy switching.[5] Filamentary RRAM is a metal/oxide/metal device that operates by forming single or multiple filaments composed of oxygen vacancies created by a soft breakdown in the oxide due to the applied electric field.[6] One of the challenges for filamentary RRAM to switch gradually across a large range of conductance values is the abrupt set process.[7] The filament formation and the subsequent set and reset cycles are due to O^{2-} ion movement between the filament and the top electrode (TE), which serves as the oxygen reservoir. In HfO_x RRAM, the O^{2-} ion movement is mostly driven by the electric field (E-field) due to its relatively low hopping activation energy (0.7 eV).[8] The E-field driven ion movement causes a soft oxide breakdown which initiates rapid positive feedback of current and local self-heating, making the set process abrupt.[8]

However, it has been demonstrated that O^{2-} diffusion is thermally controlled, where both the lateral temperature gradient away from the filament and the high temperature of the filament increase the lateral diffusion of O^{2-}.[8,9] Padovani *et al.* demonstrated by kinetic Monte Carlo modeling that high temperature formation causes a wider filament.[8] Trap-assisted tunneling transport between the oxygen vacancies in a wider filament result in multiple stable conduction paths through the filament resulting in a gradual and linear change in resistances.[10] High temperature operation of the RRAM device, as performed by Jiang *et al.*,[9] requires a separate micro-thermal stage that is not scalable. This approach also cannot directly probe temperature

gradients at nanoscale resolution due to fabrication constraints. In addition, probing the surrounding oxide may not be sufficient to get a complete thermal picture of the filament, since most of the heat is dissipated through the electrodes. Note that the filament typically ruptures and reforms at the top electrode interface. Adding a thermal barrier material with low thermal conductivity and high electrical conductivity between the switching oxide and the bottom electrode (BE) could raise the temperature in the switching layer without reducing the E-field within the filament, thereby increasing lateral diffusion of O^{2-} ions to form a wider filament.

Wu *et al.*[11] reported thermal enhancement using a conductive TaO_x layer between HfO_x and the BE, where the gradual switching range from the high to low resistance state (HRS to LRS) is 3× and the switching is highly non-linear. However, no experimental visualization of the wider filament caused by the TaO_x thermal barrier has been reported. The TaO_x thermal conductivity is relatively high ($\sim 10\,W\,m^{-1}\,K^{-1}$)[11] compared to HfO_x (~ 0.5 to $1.0\,W\,m^{-1}\,K^{-1}$).[12] Therefore, the origin of gradual resistive switching from TaO_x insertion could be due to the additional thermal interfaces (electrode/TaO_x and TaO_x/HfO_x) and the low oxygen vacancy mobility of TaO_x compared to HfO_x[13] which could also result in effective width modulation of the conductive filament.[7]

In this work, we report experimental visualization of a conductive filament and correlate its morphology with the switching characteristics including on/off ratio, set voltage, and gradual switching behavior. Our experiments suggest that the filament is wider in HfO_x RRAM with a $Ge_2Sb_2Te_5$ (GST) thermal barrier placed between HfO_x and the BE. We choose GST here because such chalcogenide glasses have lower thermal conductivity ($\sim 0.45\,W\,m^{-1}\,K^{-1}$ in the fcc phase)[14] and higher electrical conductivity than transition metal oxides such as HfO_x and TaO_x. We have observed that for similar input power, the HfO_x + GST devices show 1.5–2× higher temperature difference at the filament hot spot with respect to the ambient. This reduces the set voltage and results in a linear and gradual resistive switching due to thermal enhancement in this RRAM device.

Our RRAM is fabricated in series with an NMOS Si transistor to form a 1-transistor 1-resistor (1T1R) test structure. Figures 1(a) and 1(b) show a schematic of the RRAM cross section and the fabrication flow, respectively, and Fig. 1(c) shows the top-side optical image of the completed 1T1R. The transistor has gate length $L = 5\,\mu m$ and width $W = 5\,\mu m$. After the transistor is fabricated, the drain contact is extended to form the BE (50 nm Pt) of the RRAM, followed by a layer of sputtered GST (12 nm) on the BE. The GST region ($5\,\mu m \times 5\,\mu m$) is patterned using a liftoff process to fully cover the BE ($500 \times 500\,nm^2$ and $1 \times 1\,\mu m^2$) sidewalls. A very thin capping layer of Hf (1 nm) is sputtered *in situ* to prevent the oxidation of the GST, and the thin Hf film oxidizes to HfO_x upon vacuum break. The HfO_x (5 nm) switching layer is then deposited by atomic layer deposition (Cambridge Nanotech Savannah S200) at 200 °C, using TDMA-Hf as the Hf precursor and water as the oxygen source. Finally, the TE is sputtered and patterned as TiN (30 nm) capped by Pt (10 nm) to make a crossbar structure. Both $500 \times 500\,nm^2$ and $1 \times 1\,\mu m^2$ size devices were fabricated on the same die. Due to the processing temperature of HfO_x, the as-deposited amorphous GST crystallizes into the cubic (fcc) phase.

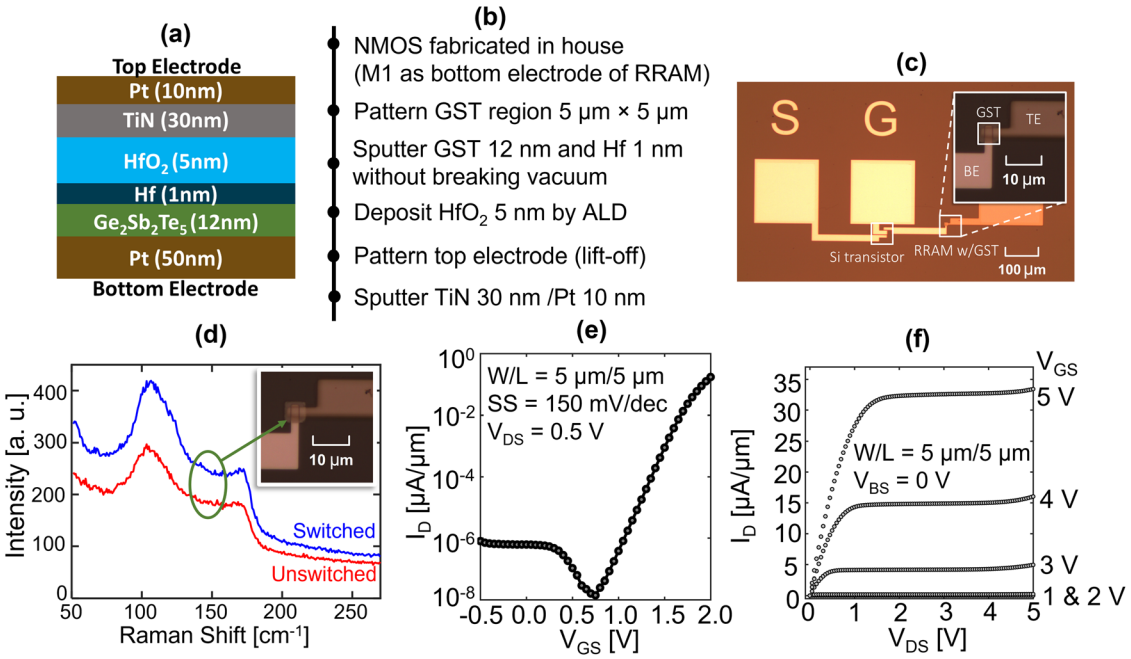

FIG. 1. (a) Device cross section, (b) fabrication flow, and (c) optical image of the 1T1R structure. S and G correspond to the source and gate of the access transistor. Note that the GST region extends slightly beyond the crossbar area to cover the bottom electrode sidewall. (d) Raman spectra of the GST adjacent to the crossbar, indicating crystalline GST both before and after switching. We observe a slight change in the spectra after switching. Inset displays an optical image with the arrow pointing to the spot where Raman measurements were done. (e) Measured I_D vs V_{GS} showing subthreshold slope (SS) = 150 mV/dec and (f) I_D vs V_{DS} characteristics of the transistors in the 1T1R structure.

In Fig. 1(d), we observe that after switching, the Raman spectra show a slightly asymmetric peak at ~100 cm^{-1} which indicates some mixed phase other than fcc.[16]

The devices undergo RRAM forming with a linear bipolar DC–voltage (I–V) sweep up to 6 V while keeping the BE at 0 V. During the forming process, the compliance current is controlled by the 1T1R transistor gate voltage. The I_D vs V_{GS} and the I_D vs V_{DS} characteristics of the NMOS transistor are shown in Figs. 1(e) and 1(f), respectively. We measure the apparent changes in the width of the filamentary region with multiple steady-state voltage biases using scanning thermal microscopy (SThM),[15] a scanning probe technique which enables temperature measurement of the RRAM top surface with sub-100 nm spatial resolution.[15,16] The detailed parameters of the SThM measurement are reported in a separate publication.[15]

Figure 2(a) shows the SThM tip voltage (V_{SThM}, proportional to the surface temperature rise) across the top surface, for devices with only HfO_x and those with HfO_x + GST, at several bias conditions. These devices were formed and cycled five times to the LRS before measurement. During measurement, a low magnitude, steady-state bias is applied such that the filament conducts a current small enough to not disturb it, but large enough to cause static temperature-rise by self-heating which is detected by the SThM on the top surface. Figures 2(a-i) and 2(a-ii) show the SThM tip voltage map for zero current flowing through the filament. This figure establishes the baseline measurement that represents the topography of the device surface. At a smaller current level, driving 20–30 μW through the filament, we start to observe the increase in V_{SThM} [Figs. 2(a-iii) and 2(a-iv)], indicating Joule heating. When the power reaches 55–70 μW [Figs. 2(a-v) and 2(a-vi)], a hot spot is seen with the highest V_{SThM}, representing the possible location of the filament. Figure 2(b) shows the estimated ΔT at the top of the device, after calibration of V_{SThM} from known temperatures.[15] (This temperature corresponds to the highest V_{SThM} point in the 2D map.)

We observe that the HfO_x + GST device has higher peak hot spot temperature rise (ΔT, which is proportional to V_{SThM}), indicating better heat trapping due to the lower thermal conductivity of the GST thermal barrier. The temperature rise at the top surface for the same electrical power is as much as twice in our RRAM device with GST, compared to control devices without, at similar applied electrical power. Figure 2(c) shows the line profile of ΔT as a function of the x-axis [in Fig. 2(a)] through the hot spot. The broader hot spot in HfO_x + GST RRAM is due to the higher thermal resistance of the HfO_x + GST stack, which results in a higher temperature rise for the same applied power compared to the GST-only device [Fig. 2(b)]. This suggests that GST with its lower thermal conductivity acts as a thermal barrier which prevents heat loss from the switching layer (HfO_x) to the BE. During the forming, the field-assisted bond breaking increases local electrical conductivity, which increases local heating and eventually triggers a thermal runaway. Thermal enhancement using a low thermal conductivity material allows more heat to flow laterally and the filamentary hot spot to become wider, causing a higher peak temperature than without the thermal barrier. According to a kinetic Monte Carlo simulation, the Coulomb repulsion between the O^{2-} ions, combined with high temperature, causes the oxygen ions to migrate more radially.[8] This results in oxygen vacancies to distribute

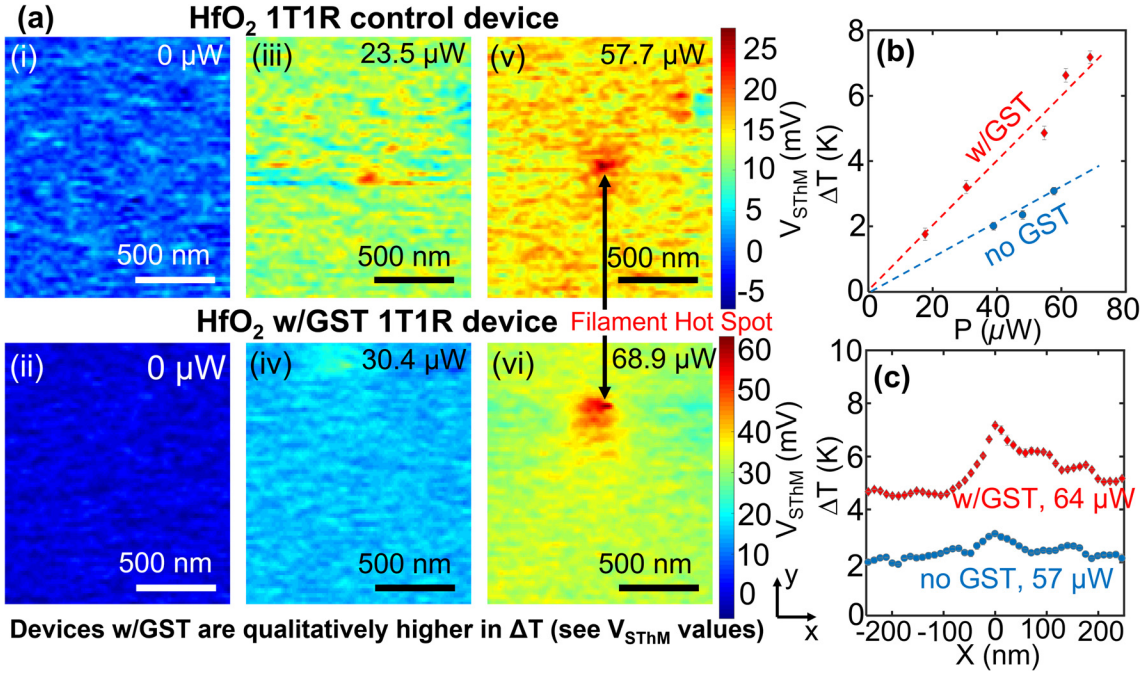

FIG. 2. (a) Scanning thermal microscopy (SThM) imaging of the 1T1R devices after filament formation. Top row (i, iii, v) shows a control device with only HfO_x and bottom row (ii, iv, vi) shows a HfO_x + GST device. The current is kept constant during scanning to ensure the filament conducts, making it visible through the top-side hot spot. Devices with GST have qualitatively higher temperature rise (ΔT), which is directly proportional to the measured V_{SThM} values. (b) Peak temperature at the hot spot relative to the ambient temperature as a function of input power during the scanning. Note that the rate of heating in the HfO_x + GST device is 1.5× to 2× that of HfO_x device, (c) measured temperature profile at the hot spot for a certain power, showing broadening of the hot spot. This demonstrates widening of the filament.

more sparsely, forming a wider filament. In the HfO_x-only device, filament formation is dominated by the E-field, which causes vertical movement of the O^{2-} ions to the top electrode and results in a narrower, more compact filament.

In order to understand the differences in charge transport between the two types of devices, we plot the quasi-static current–voltage switching characteristics in Fig. 3(a), where each device is cycled 50 times between set and reset after forming. Figure 3(b) shows the comparison of the LRS and HRS distributions for both HfO_x-only and HfO_x+GST devices over the 50 switching cycles extracted from Fig. 3(a). We observe higher on/off ratio and cycle-to-cycle variation (specifically HRS state) in HfO_x + GST device compared to HfO_x-only device. Compact distribution of vacancies in a HfO_x-only RRAM ensures Ohmic-like conduction through the filament during the reset. This results in Joule heating which facilitates oxygen motion and their recombination with vacancies. In devices with a thermal barrier, larger Joule heating gives rise to sharp reset transition in quasi-static mode, unlike HfO_x-only device where gradual transition from LRS to HRS is observed. The impact of Joule heating can be further confirmed by applying a lower reset stop voltage ($V_{rst} = -1.5$ V) at a lower compliance current (50 μA) (Fig. S1 of the supplementary material) in HfO_x + GST device. This results in a gradual reset, although with a lower on/off ratio and tighter LRS and HRS distribution. One important consequence of a wider filament is that the electron transport during the switching is sensitive to the change in average tunneling distance between the vacancies, which can change between each switching cycle due to both radial and vertical O^{2-} ion movement in devices with thermal barrier. While the resulting device can switch to many resistive states between the LRS and HRS states, it can also show significantly higher cycle-to-cycle and set voltage variation [Figs. 3(b) and 3(c)].

Importantly, even if a relatively thicker GST layer with respect to the thickness of the HfO_x layer is inserted in HfO_x + GST device, the set voltage (V_{set}) does not increase because the HfO_x is more resistive than the GST when the device is in HRS. A majority of the V_{set} voltage drop is across the oxide rather than the GST, because GST is more electrically conductive. In fact, Fig. 3(c) shows that the median V_{set} of the HfO_x + GST device is lower than that of the HfO_x device (the distribution is over 50 cycles of switching) for same reset stop voltage (V_{rst}). This also suggests that adding GST makes it easier to form a filament by heat trapping inside the HfO_x, in agreement with the findings of Jiang *et al.*[9] that forming voltage is lowered at higher temperatures. The reduction in V_{set} is more significant for higher compliance current ($I_{cc} = 100$ μA), which indicates that more heating in the filament increases the mobility of the O^{2-} ions, requiring less E-field for set.

Despite its higher cycle-to-cycle variation, the switching dynamics in the HfO_x+GST device is repeatable across multiple devices. Figure 4(a) shows the forming curve for two different devices with different areas. The forming voltages are very similar, confirming filamentary switching in these devices. Figure 4(b) shows the LRS and HRS distribution for these two devices over more than 50 cycles, confirming the repeatability of the process across multiple devices. However, device optimization for a large array and hence the extraction of device-to-device variation across many devices (~kbit to ~Mbit) is beyond the scope of this work.

We demonstrate gradual switching in HfO_x + GST RRAM by applying a pulse train with the same amplitude and width and measuring the resistance after each pulse. The comparison of the conductance as a function of the number of pulses between the HfO_x + GST and HfO_x-only devices is shown in Fig. 5. Both potentiation (low to high conductance) and depression (high to low conductance) show gradual

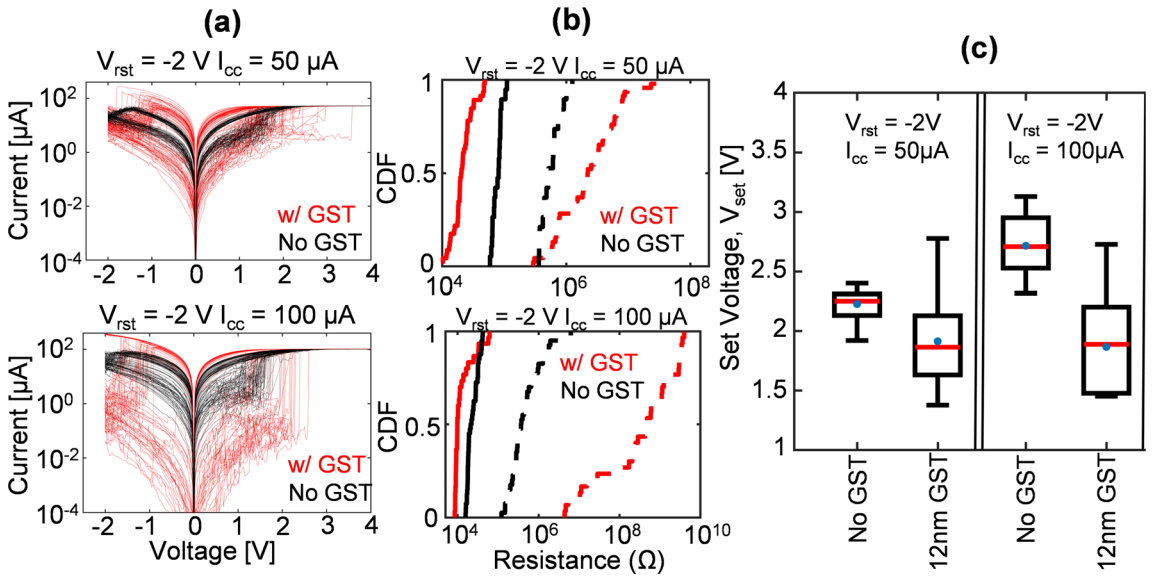

FIG. 3. (a) Comparison of current–voltage characteristics between HfO_x + GST (red lines) device and HfO_x-only device (black lines) for different compliance currents. (b) Cumulative distribution function (CDF) of LRS and HRS states measured at a read voltage of 0.1 V after each DC switching cycle of the RRAM (a), calculated over 50 switching cycles, comparing a HfO_x + GST device (red lines) with a HfO_x-only device (black lines) for different compliance currents, I_{cc}. Solid lines represent LRS and dashed lines represent HRS. Note the on/off ratio increases significantly for the HfO_x + GST device. (c) Distribution of set voltages (V_{set}) during each DC switching cycle extracted over 50 switching cycles of the RRAM, comparing a HfO_x + GST device with a HfO_x-only device for different compliance currents (I_{cc}).

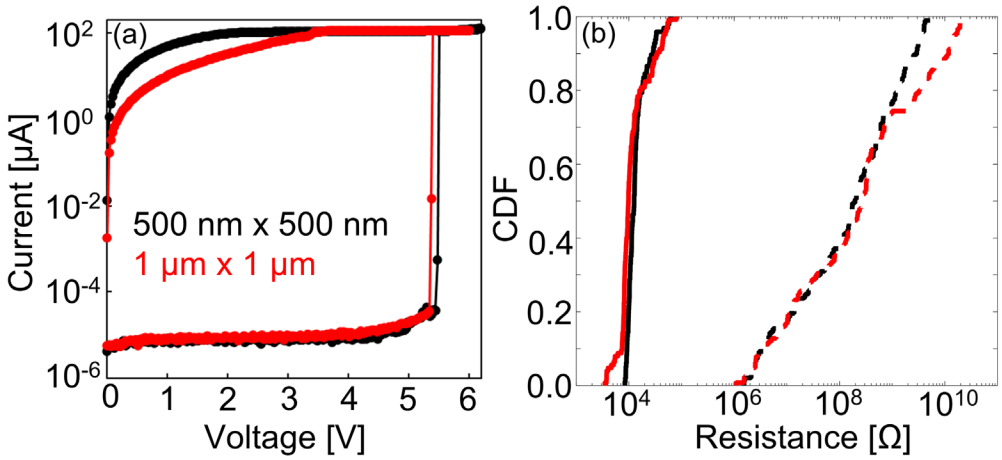

FIG. 4. (a) Forming curve comparison between 500 × 500 nm^2 (black) and 1 × 1 μm^2 (red) HfOx + GST devices. The compliance current is 100 μA. (b) Cumulative distribution function (CDF) of LRS and HRS states measured at a read voltage of 0.1 V after each DC switching cycle of the devices shown in (a), calculated over 50 switching cycles.

and linear switching with a ∼2× dynamic range in HfO_x+GST device. However, for the HfO_x-only device, the potentiation (set) is highly abrupt, and the depression (reset) is gradual but highly non-linear. This is expected for a typical HfO_x-based RRAM as reported in the literature.[7,11] Note that HfO_x + GST devices show faster switching than HfO_x-only device. In the HfO_x + GST device, for potentiation (depression), the write pulse amplitude and width are +1.8 V (−1.77 V) and 100 ns (70 ns), respectively. In both cycles, a 1 ns rise/fall time is used. The gradual switching response is linear with respect to the number of pulses applied. In the HfO_x-only device, for potentiation (depression), the write pulse amplitude and width are +2.5 V (−2 V) and 500 ns (500 ns), respectively. In both cycles, a 50 ns rise/fall time is used. The higher amplitude and longer pulse increase the conductivity range of the switching, but the same pulse amplitudes and widths used in the HfO_x+GST device, if applied to the HfO_x-only device, results in HRS and LRS to be stuck. Detailed optimization to find the smallest and fastest pulse that could reliably switch HfO_x-only device is beyond the scope of this work. However, this experiment demonstrates that heat trapping in HfO_x due to the GST thermal barrier layer causes gradual set/reset. We also uncover a trade-off between amplitude, pulse width, and the desired lowest resistance state that determines the analog switching of the RRAM and its linearity.

By incorporating GST as a thermal barrier layer, we demonstrate gradual switching of the device with one of the best linearities for bilayer RRAMs reported in the literature (Table I). Our reported nonlinearity is one order of magnitude lower for a ∼2× resistance window. We also observe a higher resistance switching window with increasing number of pulses which results in higher nonlinearity. The switching pulse amplitude and width are also among the best reported values. However, the device needs to be optimized toward higher on/off ratio

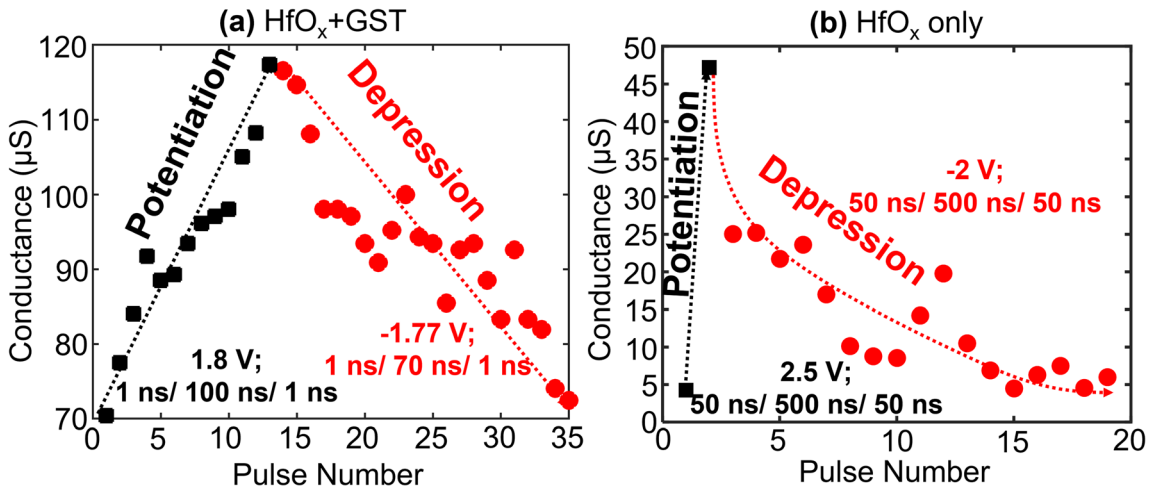

FIG. 5. Conductance vs pulse number for a sequence of identical pulses applied to the (a) HfO_x + GST and (b) the HfO_x-only 1T1R device. The pulse shapes are marked in the figure.

TABLE I. Gradual switching memory device comparison.

Type of the analog RRAM	$TiN/TaO_x/HfO_x/TiN$[11]	$Ta/TaO_x/TiO_2/Ti$[17]	$Al/Al_2O_x/HfO_x/Ti$[7]	$Pt/TiO_x/HfO_x/Ti$[18]	$TiN/HfO_x/GST/Pt$ (this work)	Ideal analog RRAM
Nonlinearity (potentiation)	0.71	0.3	0.1	0.65	0.02	0
Nonlinearity (depression)	0.67	0.36	0.1	0.94	0.01	0
Lowest resistance	36 kΩ	5000 kΩ	17 kΩ	412 Ω	8 kΩ	High
Potentiation pulse	1.6 V/50 ns	3 V/40 ms	0.9 V/100 μs	1.2 V/50 ns	1.8 V/100 ns	Low voltage/ fast pulse
Depression pulse	1.6 V/50 ns	3 V/10 ms	1 V/100 μs	1.4 V/50 ns	1.77 V/70 ns	Low voltage/ fast pulse
On/off ratio (potentiation/ depression)	3.3/2.2	2/2	2.6/3.9	2.1/3.65	1.7/1.7	Large

and higher LRS level. Using similar chalcogenide materials with a higher melting temperature and lower thermal conductivity, for example, $TiTe_2$, we can improve the thermal confinement while improving the device-to-device variation by preventing the melt-quench of the barrier layer for a broad range of pulsing conditions.

In conclusion, we have demonstrated experimental observation of filament formation in RRAM and uncovered that inserting a GST thermal barrier causes a wider filament to form in the HfO_x. Such thermally enhanced RRAMs show higher on/off ratio and highly linear gradual resistive switching. Gradual resistance switching is promoted by the formation of wider filaments (in control devices without a GST barrier, where the oxygen vacancies are more compact). Such change in the filament morphology is more sensitive to the switching pulse, where O^{2-} diffuses both vertically and horizontally reducing the bistable nature of filamentary switching. Lateral heat spreading inside the HfO_x switching material also improves the mobility of O^{2-} ions, resulting in a decrease of the set voltage, improving the energy-efficiency of switching. Such thermally enhanced RRAMs can be a potential candidate as synaptic devices for in-memory computing.

See the supplementary material for quasi-static current voltage characteristics and the LRS and HRS distributions of the $500 \times 500\,nm^2$ HfO_x + GST device where the compliance current is set at 50 μA with a reset stop voltage set at −1.5 V (Fig. S1).

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Raisul Islam: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review and editing (equal). **H.-S. Philip Wong:** Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – original draft (supporting); Writing – review and editing (supporting). **Shengjun Qin:** Investigation (supporting); Methodology (supporting); Writing – review and editing (supporting). **Sanchit Deshmukh:** Data curation (supporting); Formal analysis (supporting); Investigation (supporting); Methodology (supporting); Visualization (supporting); Writing – original draft (supporting); Writing – review and editing (supporting). **Zhouchangwan Yu:** Investigation (supporting); Methodology (supporting); Writing – review and editing (supporting). **Cagil Koroglu:** Investigation (supporting); Methodology (supporting). **Asir Intisar Khan:** Data curation (supporting); Investigation (supporting); Methodology (supporting); Writing – review and editing (supporting). **Kirstin Schauble:** Investigation (supporting); Methodology (supporting). **Krishna C. Saraswat:** Funding acquisition (equal); Supervision (equal); Writing – review and editing (supporting). **Eric Pop:** Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – original draft (supporting); Writing – review and editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supplementary Material

Improved Gradual Resistive Switching Range and 1000× On/Off Ratio in HfO_x RRAM Achieved with a $Ge_2Sb_2Te_5$ Thermal Barrier

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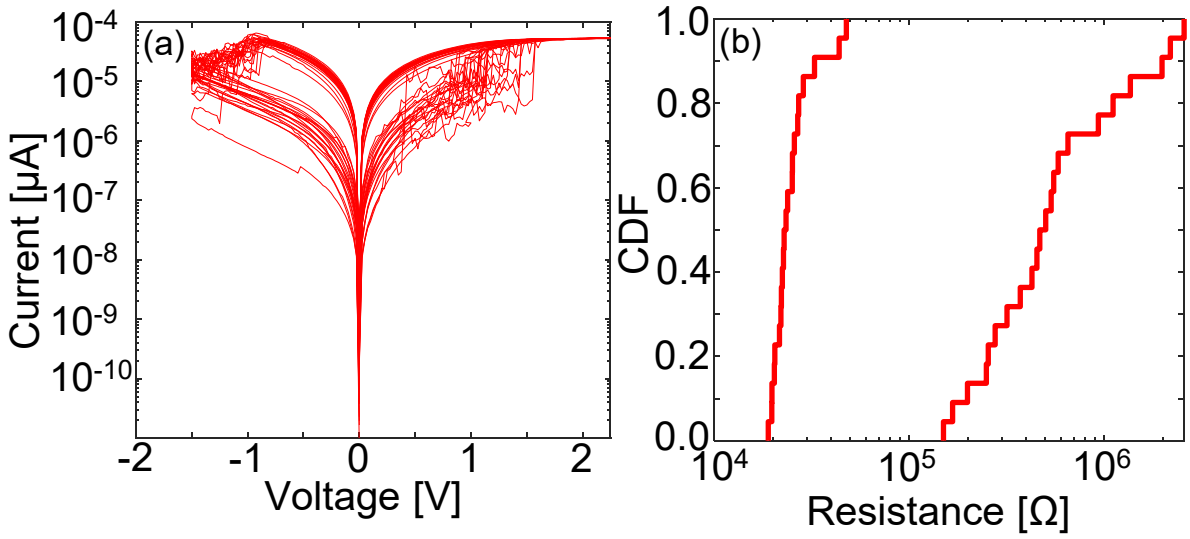

FIG. S1. (a) Quasi-static current-voltage characteristics of 500 nm × 500 nm HfOx+GST RRAM for 25 switching cycles having a compliance current, I_{cc} = 50 μA and reset stop voltage, V_{rst} = -1.5 V. Note that all the reset cycles show gradual transition. (b) Cumulative distribution function (CDF) of the LRS and HRS states measured at a read voltage of 0.1 V after each DC switching cycle extracted from Fig. S1 (a). The cycle-to-cycle variation at the HRS state is smaller than that shown in Fig. 3(b) for the same device.