Improved Hysteresis and Reliability of MoS_2 Transistors With High-Quality CVD Growth and Al_2O_3 Encapsulation

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***Abstract*— We report considerable improvement in the hysteresis and reliability of single-layer MoS_2 field-effect transistors (FETs) achieved by chemical vapor deposition (CVD) of MoS_2 and dielectric encapsulation. Our results show that a high-quality 15-nm thick Al_2O_3 layer allows for an efficient protection of the devices from adsorbent-type trapping sites. Combined use of the CVD-grown MoS_2 as a channel and encapsulation simultaneously leads to at least an order of magnitude smaller hysteresis and up to two orders of magnitude lower long-term drifts of the transistor characteristics. Together with high on/off current ratios ($\sim 10^9$) achieved in our devices, this presents a considerable advance in the technology of MoS_2 FETs. As such, we conclude that both CVD growth of MoS_2 and encapsulation present important technological steps toward reaching commercial quality standards of next-generation two-dimensional (2D) material technologies.**

***Index Terms*— Single-layer MoS_2, encapsulation, reliability, charged traps, hysteresis, bias-temperature instabilities.**

I. Introduction

MOLYBDENUM disulfide (MoS_2) is now considered a promising "beyond-graphene" material for applications in next-generation two-dimensional (2D) electronics. In contrast to graphene, MoS_2 has a sizable direct electronic bandgap of up to ~2.6 eV in the single-layer limit [1]–[3], which makes this material attractive for digital device applications. Owing to this, considerable progress in fabrication of single-layer (1L) MoS_2 field-effect transistors (FETs) has been demonstrated recently. In particular, numerous single-layer devices with SiO_2 [4], [5], Al_2O_3 [6], HfO_2 [4] and hexagonal boron nitride (hBN) [7], [8] gate insulators have been reported. The typical on/off current ratios of these devices are within 10^5–10^7, while the subthreshold swing (SS) can reach nearly ideal values down to 74 mV/dec, as already reported for high-k/MoS_2/SiO_2 devices [4]. In addition, a number of successful attempts at fabricating multi-layer MoS_2 FETs have been undertaken [9]–[17], with the best subthreshold swing of 69 mV/dec achieved for MoS_2/high-k devices [17]. However, independent of the number of channel layers, available MoS_2 device prototypes often suffer from a sizable hysteresis [5], [8], [10], [14], [15] and long-term drifts of the gate transfer characteristics [8], [11], [13], which are known from Si technologies as bias-temperature instabilities (BTI) [18]–[20]. These issues are typically attributed to charge trapping by both oxide traps [8], [13], [15] and adsorbent-type trapping sites (e.g. water molecules) on the MoS_2 channel [5], [8], [10], [11]. While the hysteresis and BTI impede stable device operation at a defined operating point, the reliability of MoS_2 prototypes with respect to these issues is still far below the standards of modern commercial FETs [8], [11], [13]. As such, BTI and hysteresis in MoS_2 FETs must be addressed prior to commercialization of these next-generation technologies.

Here we report on the improvement of both the reliability and the performance of 1L MoS_2 FETs with SiO_2 insulator by optimized device processing and encapsulation with a high-quality 15 nm thick Al_2O_3 layer. Our results show that these devices not only exhibit high on/off current ratio ($\sim 10^9$), but also that both the hysteresis and the threshold voltage shifts due to positive and negative BTI (PBTI and NBTI, respectively) become 1–2 orders of magnitude smaller. Combined with the use of CVD-grown MoS_2, this presents a considerable breakthrough in the technology of 2D single-layer materials and devices.

II. Devices

Our devices are single-layer back-gated MoS_2 FETs with a 25 nm thick SiO_2 insulator, 50 nm thick gold source/drain contacts and a 15 nm thick high-quality Al_2O_3 encapsulation (Fig. 1a,b). Single-layer MoS_2 was grown at $T = 850$ °C in Ar atmosphere (760 Torr) by chemical vapor deposition (CVD) directly on $SiO_2/p^{++}-Si$ substrates [21]; growth time was 15 minutes. Then, after verification of the superior quality of our CVD-grown MoS_2 film [22], the MoS_2 FETs were fabricated via a three-step optical lithography process to

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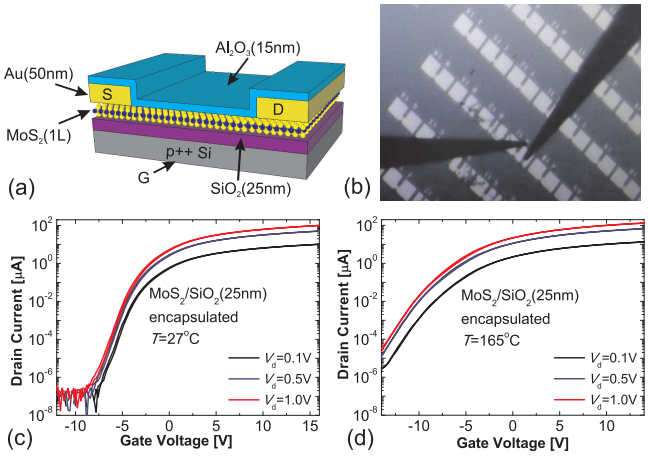

Fig. 1. (a) Schematic layout of our CVD-grown 1L MoS_2 FETs encapsulated by a 15 nm thick Al_2O_3 layer. (b) Optical microscope image of the investigated devices (the contact pads are $100 \times 100\,\mu m^2$). The $I_D - V_G$ characteristics of our device ($L = 8\,\mu m$, $W = 20\,\mu m$) measured at $T = 27°C$ (c) and $T = 165°C$ (d).

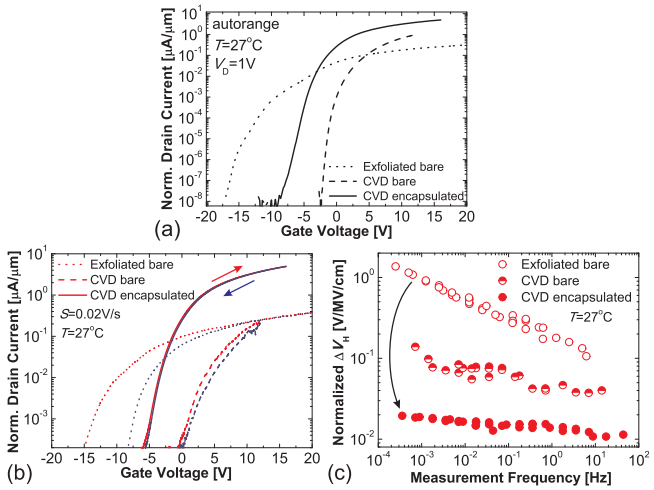

Fig. 2. (a) The $I_D - V_G$ characteristics of exfoliated MoS_2/SiO_2(90 nm) FET ($L = 1.5\,\mu m$, $W = 7\,\mu m$) and CVD-grown MoS_2/SiO_2(25 nm) devices ($L = 6\,\mu m$, $W = 10\,\mu m$ for bare and $L = 8\,\mu m$, $W = 20\,\mu m$ for encapsulated device) measured using the autorange mode. The current is normalized by W. (b) The $I_D - V_G$ characteristics of the same devices measured using both sweep directions and a constant sweep rate $S = 0.02$ V/s. (c) The normalized hysteresis widths versus the measurement frequency f.

simultaneously create hundreds of devices with channel dimensions ranging from 2 to 20 μm [22]. First, probe pad areas were defined with photoresist, etched out with O_2 plasma and filled with 2/40 nm Ti/Au. Following liftoff, contact extension regions were defined and filled with 50 nm of pure Au, in order to minimize contact resistance [23]. After a second liftoff, the channel widths were defined and the exposed MoS_2 was etched away with O_2 plasma, followed by a solvent clean to remove the photoresist. Finally, a high-quality Al_2O_3 encapsulation layer was deposited using a modified method of [24]. Namely, 120 cycles of atomic layer deposition (ALD) of Al_2O_3 were performed at 300 °C after deposition of a 1.5 nm thick Al nucleation layer. Note that a relatively high ALD growth temperature allows to remove impurities that might be present on the surface of the MoS_2 channel before deposition of the encapsulation layer. This Stanford-built ALD setup allows to deposit a high-quality Al_2O_3 layer with few inherent charge traps.

III. Experimental Details

Electrical measurements were performed in a vacuum ($\sim 5 \times 10^{-6}$ Torr) in complete darkness. This was necessary to obtain consistent results for comparison with bare devices which are known to be sensitive to the detrimental impact of environment [5], [10]. First, we measured the drain current vs. gate voltage ($I_D - V_G$) characteristics using the autorange mode, which was necessary to evaluate the best case on/off current ratio in our devices. Then we analyzed the hysteresis dynamics by measuring the $I_D - V_G$ characteristics using forward (V^+) and reversed (V^-) sweep directions and different measurement frequencies $f = 1/(Nt_{step})$, with N being the number of V_G steps and t_{step} the sampling time [8]. Finally, we examined the BTI degradation and recovery dynamics using our experimental technique by applying subsequent stress/recovery cycles with logarithmically increased stress times t_s [8], [25]. A considerable difference compared to our previous work for MoS_2 FETs [8] is that, similarly to the technique used for Si devices [26], here a constant gate voltage is applied not only during stress (V_{GS}), but also during recovery (V_{GR}). This leads to more reproducible results, as otherwise the potential at the back gate, which is formed by the Si substrate, shows large uncontrollable drifts.

IV. Results and Discussion

In Fig. 1c we show the $I_D - V_G$ characteristics measured for our encapsulated CVD-grown MoS_2 device at $T = 27$ °C. The on/off current ratio is at least 10^9, which is larger than previously reported for CVD-grown MoS_2. Also, similarly to our previous work on bare exfoliated MoS_2 FETs [8], at $T = 165$ °C (Fig. 1d) the threshold voltage V_{th} of the same device becomes more negative. However, here this issue is less pronounced and thus the measured on/off current ratio remains as high as 10^7, which further underlines the high stability of these encapsulated CVD-grown devices.

In Fig. 2a, b we compare the $I_D - V_G$ characteristics measured for our encapsulated CVD-grown MoS_2/SiO_2(25 nm) devices, bare devices fabricated using the same method, and bare exfoliated single-layer MoS_2/SiO_2(90 nm) FETs which are similar to those studied in our previous work [8]. Owing to improved processing technology, CVD-grown devices exhibit considerably steeper subthreshold slopes and larger on current values. Furthermore, the hysteresis, which is sizable for bare exfoliated devices, becomes considerably smaller for bare CVD-grown devices and can be almost completely suppressed for their encapsulated counterparts. In Fig. 2c we compare the hysteresis widths ΔV_H normalized by the oxide field factor $(V_{Gmax} - V_{Gmin})/d_{ox}$, with d_{ox} being the oxide thickness, versus the measurement frequency f for three devices. Clearly, the encapsulated CVD-grown device exhibits nearly one order of magnitude improvement compared to a bare device of the same technology and two orders of magnitude compared to the exfoliated bare device. As such, we can conclude that our high-quality Al_2O_3 encapsulation layer efficiently protects the devices from fast adsorbent-type trapping sites which are in part responsible for the hysteresis in MoS_2 FETs.

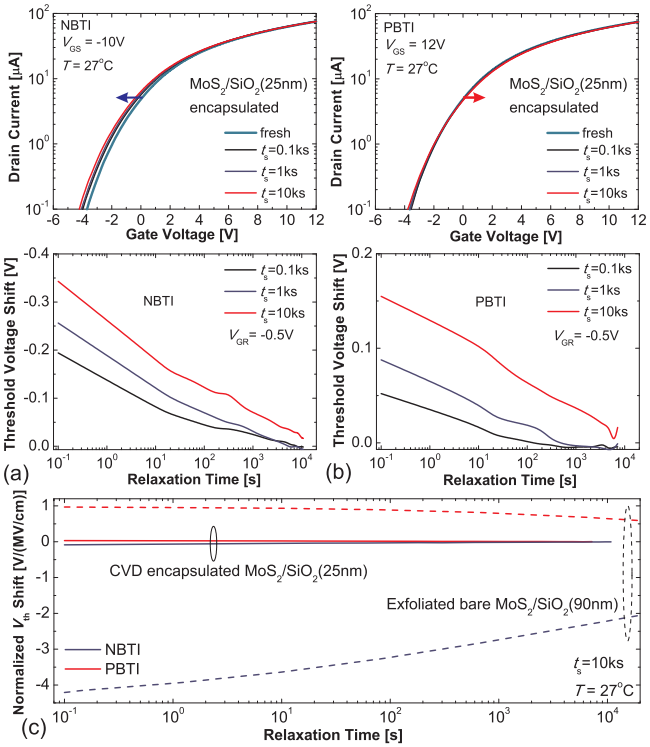

Fig. 3. Evolution of the $I_D - V_G$ characteristics of our encapsulated CVD-grown MoS_2 FET with $L = 8\,\mu$m, $W = 20\,\mu$m (top) and the corresponding V_{th} recovery traces (bottom) after subsequent NBTI (a) and PBTI (b) stresses. (c) Normalized NBTI and PBTI recovery measured after $t_s = 10$ ks stresses.

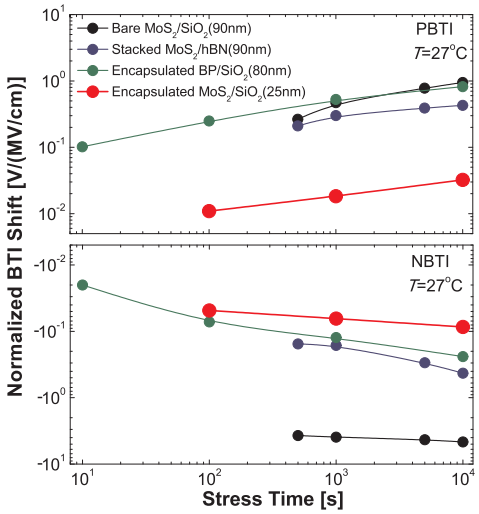

Fig. 4. Comparison of the PBTI (top) and NBTI (bottom) shifts normalized by the oxide field (0.4–4.8 MV/cm) for different 2D technologies. Encapsulated CVD-grown MoS_2/SiO_2 FETs exhibit the best NBTI and PBTI reliability.

In Fig. 3a,b we show evolution of the $I_D - V_G$ characteristics and corresponding V_{th} recovery traces measured at the recovery gate voltage $V_{GR} = -0.5$ V after subsequent NBTI and PBTI stresses. Remarkably, the degradation is considerably smaller than has been ever reported for MoS_2 FETs. In particular, in Fig. 3c we compare the NBTI and PBTI recovery traces measured after stresses with $t_s = 10$ ks for our encapsulated CVD-grown MoS_2 FETs and their bare exfoliated counterparts from our previous work [8]. Since the oxide thicknesses and stress voltages are different, we normalize the threshold voltage shifts by the oxide field $F_{ox} = V_{GS}/d_{ox}$, which is 2.2 MV/cm for exfoliated device and either 4 MV/cm (NBTI) or 4.8 MV/cm (PBTI) for CVD-grown MoS_2 FET. While for encapsulated CVD-grown devices both NBTI and PBTI shifts are more than an order of magnitude smaller, they tend to completely recover after several hours. In contrast, the degree of recovery of considerable BTI shifts in bare exfoliated MoS_2 FETs for the same time interval does not exceed 40%. Therefore, we conclude that Al_2O_3 encapsulation, together with our optimized device processing, allows to minimize the amount of slower process-induced defects and adsorbents, which may contribute to charge trapping leading to BTI. As such, we suggest that the observed BTI degradation in our encapsulated devices is dominated by oxide traps in SiO_2, which are situated within several nanometers from the MoS_2/SiO_2 interface and thus can exchange charges with the channel by means of tunneling. As known from Si technologies [27] and our previous works on black phosphorus (BP) [28] and MoS_2 FETs [29], these defects are energetically aligned within certain defect bands, with the one contributing to charge trapping in MoS_2 FETs located ~2.7 eV below the SiO_2 conduction band edge [27], [28]. This position of the defect band relative to the MoS_2 conduction band, together with the Fermi level pinning in accumulation [30], [31], makes NBTI more favorable than PBTI. That is why PBTI degradation in our devices is weaker than NBTI, which is important for MoS_2 n-FETs working at positive V_G.

Finally, in Fig. 4 we compare initially measured normalized PBTI and NBTI shifts versus t_s for our encapsulated CVD-grown MoS_2/SiO_2 FETs with those obtained for bare exfoliated MoS_2/SiO_2 [8], stacked MoS_2/hBN [8] and BP/SiO_2 [28] devices. Remarkably, the PBTI shifts for our encapsulated MoS_2 FETs are around an order of magnitude smaller than in previously studied 2D devices. As for NBTI, encapsulated MoS_2 devices studied here can slightly outperform Al_2O_3 encapsulated BP/SiO_2 FETs, which have been previously considered the most stable with respect to room temperature BTI among other 2D devices. Although commercial standards require further improvement of the reliability by at least one order of magnitude, our encapsulated MoS_2 FETs present a considerable step forward in this direction.

V. Conclusions

In summary, we have suggested a versatile way to improve both the reliability and performance of MoS_2 FETs by optimization of the device processing conditions and the use of a high-quality Al_2O_3 encapsulation to protect the devices from adsorbent-type trapping sites. While already having an extremely high on/off current ratio of ~10^9, our devices also exhibit a considerable improvement in terms of hysteresis and BTI stability. As such, we conclude that high-quality encapsulation of MoS_2 FETs, together with CVD growth of MoS_2 film, present an important technological step toward reaching commercial quality standards of these new technologies.

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