Gigahertz Integrated Graphene Ring Oscillators

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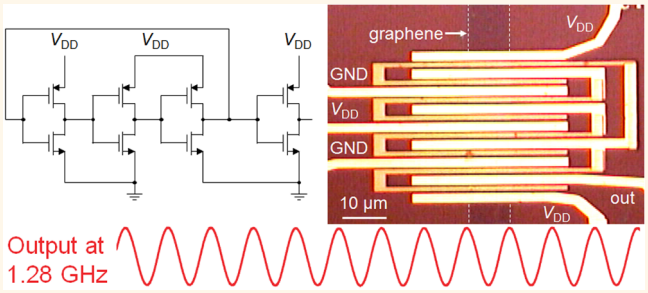
ABSTRACT Ring oscillators (ROs) are the most important class of circuits used to evaluate the performance limits of any digital technology. However, ROs based on low-dimensional nanomaterials (*e.g.*, 1-D nanotubes, nanowires, 2-D MoS_2) have so far exhibited limited performance due to low current drive or large parasitics. Here we demonstrate integrated ROs fabricated from wafer-scale graphene grown by chemical vapor deposition. The highest oscillation frequency was 1.28 GHz, while the largest output voltage swing was 0.57 V. Both values remain limited by parasitic capacitances in the circuit rather than intrinsic properties of the graphene transistor components, suggesting further improvements are possible. The fabricated ROs are the fastest realized in any low-dimensional nanomaterial to date and also the least sensitive to fluctuations in the supply voltage. They represent the first integrated graphene oscillators of any kind and can also be used in a wide range of applications in analog electronics. As a demonstration, we also realized the first stand-alone graphene mixers that do not require external oscillators for frequency conversion. The first gigahertz multitransistor graphene integrated circuits demonstrated here pave the way for application of graphene in high-speed digital and analog circuits in which high operating speed could be traded off against power consumption.



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Rapid progress of wireless, fiber-optic, and space communications has led to a growing need for digital systems capable of operating at extremely high frequency (EHF; f > 100 GHz) and signal processing at extremely high data transfer rates (>100 Gbit/s).[1] To this end, a special class of ultra-high-speed digital circuits has been developed in order to perform data conversion at the transmitting/receiving side of serial EHF lines, such that information carried by EHF digital signals can be processed at lower clock rates by low-power, highly integrated, and parallel Si complementary metal oxide semiconductor (CMOS) logic.[2] Graphene[3] could emerge as a possible contender in the ultra-high-speed circuit arena due to its very large charge carrier mobility.[4−6] Unlike other materials, the graphene mobility is equal between electrons and holes and much greater than that of InP, which currently dominates high-speed electronics.[1] The absence of a band gap in graphene, which represents a disadvantage in low-power digital applications, does not necessarily hinder high-speed circuits that achieve fast operation at the expense of a large static power dissipation and with reduced circuit complexity.[7] The power dissipation of graphene logic gates is similar to those of the fastest InP emitter coupled logic (ECL) gates,[2,8] even though graphene logic gates have larger voltage swing (as a fraction of supply voltage) than ECL gates.[9] However, only through further technological advances, some of which will be discussed here, may graphene be able to compete with or replace InP in EHF circuits.

Despite the high intrinsic cutoff frequency (f_T > 100 GHz) of individual graphene field-effect transistors (FETs),[10] no demonstrations exist yet of high-speed graphene digital circuits. This apparent discrepancy occurs

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because f_T is a measure of internal transistor delays rather than functionality in realistic electronic circuits. Logic gates, as almost all electronic circuits, require FETs with intrinsic voltage gain $A = g_m/g_d > 1$, where g_m is transconductance and g_d is output conductance. Overunity intrinsic gain at room temperature has recently been demonstrated in monolayer graphene FETs incorporated in analog voltage amplifiers[10−12] and digital inverters.[9] Voltage gain larger than unity is needed in logic gates in order to match their input and output signals. Matching allows cascading of logic gates[9] and realization of more complex, realistic circuits, of which the most important class are digital ring oscillators (ROs). ROs are composed of an odd number of inverters (each with two FETs) cascaded in a loop, which provides negative feedback at low frequencies but positive feedback at higher frequencies. The loop makes the RO unstable and therefore induces oscillation at higher frequencies, but only if the inverters satisfy stringent criteria. Each inverter in the loop must be identical, exhibiting overunity voltage gain and in/out signal matching. Moreover, the two FETs in each inverter must exhibit very low on-state resistance to be able to quickly charge/discharge the gate capacitance of the next stage. Since the oscillation frequency $f_o < f_T$ is a direct measure of delays in realistic scenarios, ROs are the standard testbeds for evaluating ultimate performance limits and the highest possible clock rates of digital logic families.[13]

ROs made from strictly low-dimensional materials have previously been demonstrated with carbon nanotubes (CNTs)[14,15] and exfoliated bilayer MoS_2,[16] but not with graphene. In the case of both CNTs and MoS_2, the oscillation frequency was limited by parasitic capacitances and by relatively large on-state resistances of the FETs (>100 kΩ), which limited the oscillation frequencies to 52 MHz (CNTs)[15] and 1.6 MHz (bilayer MoS_2).[16] On the other hand, graphene exhibits large mobility and can be processed by simple fabrication methods on a wafer scale.[17,18] Here we demonstrate high-frequency operation of ROs fabricated from wafer-scale monolayer graphene. The low resistance of graphene FETs (<624 Ω) ensured the highest oscillation frequency (f_o = 1.28 GHz) demonstrated to date in novel low-dimensional materials. The fabricated ROs also represent the first gigahertz multitransistor graphene integrated circuits, which demonstrate the potential for large-scale integration of graphene electronic devices.

RESULTS AND DISCUSSION

A schematic of the investigated ROs is shown in Figure 1a. Graphene monolayers (see Methods) were grown by chemical-vapor deposition (CVD).[19] The ROs were fully integrated on the monolayers (Figure 1b). Complementary operation of the graphene inverters within a RO is obtained between the Dirac points of the two FETs,[20] after the supply voltage $V_{DD} > 0$ is applied.[21] In this configuration, the input and output voltages at the highest-gain (*i.e.*, threshold) point of an inverter are mismatched by $V_{IN} - V_{OUT} = V_0$, where V_0 is the voltage at the Dirac point of the unbiased FETs.[9] A positive voltage at the Dirac point (V_0 > 0.2 V, measured in air at room temperature) was found in all fabricated FETs, stemming from p-type doping introduced by ambient impurities adsorbed on graphene.[3,22] Since in/out mismatch at the threshold point rapidly reduces voltage swing in multistage graphene circuits,[9] a positive back-gate voltage, $V_{BG} = (C_{ox}/C_{ox,BG})V_0$, was used to shift the Dirac point back to zero. Here C_{ox} and $C_{ox,BG}$ are the top-gate and back-gate capacitances per unit area, respectively ($C_{ox}/C_{ox,BG}$ = 121.2 and $C_{ox} \approx 1.4\ \mu F\ cm^{-2}$; see Supporting Information Figure S1). With the appropriate back-gate voltage, the voltage gain of such inverters at the threshold point is $|A_v| > 4$ (see Figure S2).

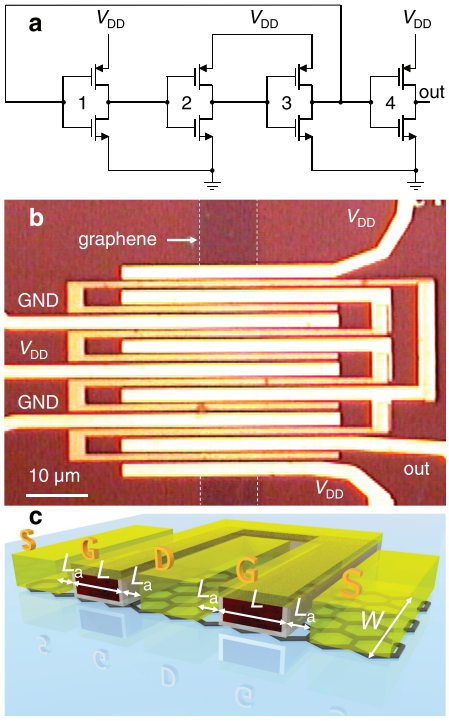

Figure 1. Integrated monolayer graphene ring oscillator (RO). (a) Circuit diagram of a three-stage RO. The RO is composed of three inverters (1−3) cascaded in a loop with the fourth inverter (4) decoupling the RO from the measurement equipment connected to the output (out). (b) Optical microscope image of a small RO (L = 1 μm and W = 10 μm) integrated on the monolayer graphene channel grown by CVD. The drain contacts of inverters 1−3 (Au; bright yellow) overlap with the gate contacts (Al/Ti/Au; orange) in order to form internal connections between the inverters. (c) Schematic of a complementary graphene inverter composed of two FETs. Source (S) and drain (D) contacts (Au; yellow) are separated by a distance L_a from the gate (G) contact (Al; red core), which is covered by an insulating layer (AlO_x; gray shell) and terminated with a conductive layer (Ti/Au; yellow). All inverters in a single RO have the same access lengths (L_a), gate length (L) and width (W). ROs were fabricated with different L and W, but in all cases the access lengths were kept constant (L_a = 0.5 μm).

Signal matching at the threshold point enables oscillations in a RO if the low-frequency voltage gain satisfies the condition $|A_v| \geq [1 + (\tan(\pi/n))^2]^{1/2}$, where n is the number of inverting stages cascaded in a loop.[23] Three-stage ROs require the highest gain ($|A_v| \geq 2$) compared to ROs with a larger number of stages ($n \geq 5$), but they also oscillate at the highest frequency. As our fabricated inverters satisfy the voltage-gain condition for $n = 3$, three-stage ROs were investigated (as shown in Figure 1) in order to reach high frequencies. The oscillation frequency of a RO depends on the gate delays of the inverters as $1/f_o = 2\sum_{i=1}^{n} \tau_i$ where τ_i is the delay of the ith inverter. Here it is assumed that FETs in an ith inverter are identical, *i.e.*, that both rise and fall time delays are equal to τ_i. In the case of a perfect (*i.e.*, symmetric) RO composed of identical inverters (without the output buffering stage, *i.e.*, inverter 4 in Figure 1a) the expression for frequency simplifies to $f_o = 1/(2n\tau) = f_{o,max}$ where $\tau_i = \tau$ is the gate delay of a single inverter. In a simple transient model (see Supporting Information Section S1) this delay is $\tau = \ln((\sqrt{5} + 1)/2)CG_D^{-1}$ where G_D is the sum of the extrinsic drain conductances of the FETs in the inverter and C is the parasitic capacitive load of the inverter. This load mostly consists of the gate capacitance of the following stage, *i.e.*, $C \approx 3C_G$, where the gate capacitance $C_G \approx LWC_{ox}$ and L and W are the gate length and width, respectively (Section S1). In order to demonstrate scaling of such circuits, we fabricated three types of graphene ROs: large ($L = 3\ \mu$m and $W = 20\ \mu$m), medium ($L = 2\ \mu$m and $W = 10\ \mu$m), and small ($L = 1\ \mu$m and $W = 10\ \mu$m). Typical values for G_D and C_G of these three types of ROs are given in the Supporting Information Table S1. With $n = 3$ and these parameter values, the simulations presented in Section S1 would lead us to expect $f_{o,max} = 457$ MHz for large ROs, $f_{o,max} = 811$ MHz for medium ROs, and $f_{o,max} = 2.08$ GHz for small ROs (Table S1).

Figure 2 shows voltage signals measured at the output of the three types of fabricated ROs with the buffering stage. In all three cases the oscillation frequencies are smaller than the respective $f_{o,max}$ because the buffering inverter introduces an additional capacitive load on the inverter to which it is connected. This additional load reduces the oscillation frequency to $f_o \approx f_{o,max} \ln(2 + \sqrt{5})/\ln(3 + 2\sqrt{2}) < f_{o,max}$ (Section S1). This yields $f_o = 359$ MHz for large ROs, $f_o = 648$ MHz for medium ROs, and $f_o = 1.76$ GHz for small ROs. The first two values are very close to the measured frequencies of 350 MHz (large RO) and 618 MHz (medium RO) shown in Figure 2. Only in the case of small ROs does the model overestimate the frequency because it does not account for all parasitic capacitances that dominate at smaller device sizes. The measured oscillation frequency scales approximately with $1/L$ mostly because G_D^{-1} does not scale with L/W due to contact resistances (which scale only with $1/W$) and the

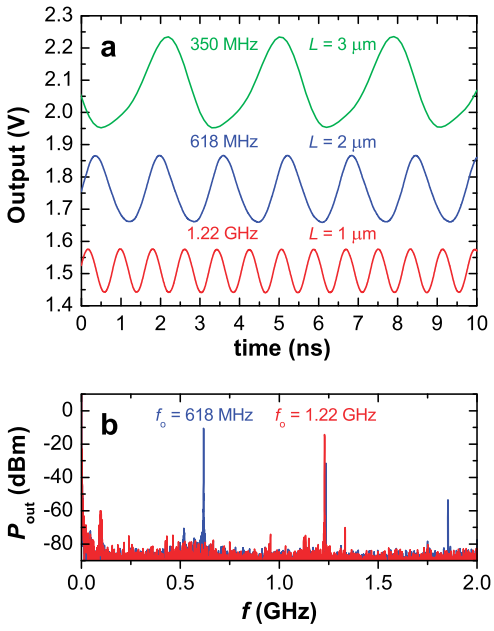

Figure 2. Output signals of buffered graphene ROs at V_{DD} = 3.5 V. (a) Large RO (green; $L = 3\ \mu$m and $W = 20\ \mu$m) oscillates at 350 MHz at V_{BG} = 34 V (see text). The voltage swing is $V_{p-p} = 0.284$ V. Medium RO (blue; $L = 2\ \mu$m and $W = 10\ \mu$m) oscillates at 618 MHz at V_{BG} = 5 V. The voltage swing is $V_{p-p} = 0.208$ V. Small RO (red; $L = 1\ \mu$m and $W = 10\ \mu$m) oscillates at 1.22 GHz at V_{BG} = 50 V. The voltage swing is $V_{p-p} = 0.136$ V. The voltage swing is strongly suppressed by the low-pass filtering of the buffer (see Sections S2, S3). The green and red curves are vertically offset for clarity, from the midpoint voltage $V_{DD}/2 = 1.75$ V. (b) Respective power spectra of the medium and small ROs. The second harmonic of the medium RO is at the position of the first harmonic of the small RO.

parasitic resistances and capacitances of the interconnects, which do not scale (statistics and scaling of the 26 working ROs are shown in Figure S9). In general, the fabricated buffered ROs exhibited oscillation frequencies in the range 284 MHz < f_o < 350 MHz (large ROs), 504 MHz < f_o < 750 MHz (medium ROs; Figure S14), and 1 GHz < f_o < 1.28 GHz (small ROs; Figure S14). The variability of f_o stems from variations in overlap resistances between the input and outputs of the inverters (which influence f_o through G_D). The largest voltage swing in fabricated ROs was 0.57 V (Section S2). All three ROs shown in Figure 2 required relatively low back-gate voltages (as low as V_{BG} = 5 V) and were operated in ambient air.

The oscillation frequency of conventional ROs, as well as those made from nanomaterials such as CNTs and MoS_2, strongly depends on the supply voltage V_{DD}. This represents a serious problem in complex digital circuits in which a large number of transistors and increased power consumption place increased demand on the voltage supply, causing it to fluctuate.[24] Such fluctuations not only have a negative impact on the operation of logic gates but also deteriorate their noise performance.[24] We found that, in contrast to other types of ROs, graphene ROs are much less

sensitive to fluctuations in the supply voltage. Figure 3 shows the power spectrum of the output signal (oscillating at $f_o \approx 700$ MHz) in a buffered RO at different supply voltages. At larger supply voltages both voltage swing and oscillation frequency are larger. Voltage swing increases with supply V_{DD} because a larger unity-gain voltage swing is obtained at larger supply voltages.[9] The increase in oscillation frequency is a consequence of an increase in the total drain conductance of graphene FETs at larger V_{DD} (as $f_o \propto G_D$). Although such a dependence of f_o on V_{DD} exists in all types of ROs, it is much weaker in the case of graphene ROs due to much weaker dependence of G_D on V_{DD} in graphene FETs (Section S4). For the RO shown in Figure 3, the change of oscillation frequency with supply voltage is $\sim$5.6%f_o/V on average. This is about 7, 21, and 51 times smaller than that of ROs based on Si CMOS (Figure S16), MoS_2,[16] and CNTs,[15] respectively. Such a weak dependence in graphene ROs could be a disadvantage in applications in which dynamic frequency and voltage scaling are used to throttle down digital circuits during periods of reduced workload. However, insensitivity of graphene ROs to power supply noise represents an important advantage in applications in which frequency stability is of the utmost importance, *e.g.*, for clock generation in high-speed digital systems.

The fabricated ROs can also be used in analog applications such as frequency mixing.[25] Graphene analog mixers[26,27] have recently been suggested as one of the possible applications of graphene in high-frequency analog electronics, since frequency mixing does not require devices that exhibit overunity voltage gain. However, without voltage gain the signals cannot be amplified (which is necessary for signal transmission), nor is it possible to generate oscillating signals. For this last reason, the graphene mixers that have so far been demonstrated[26−29] have required an external local oscillator (LO) for frequency conversion. The ROs demonstrated here can overcome these limitations and perform both modulation and generation of oscillating signals to form stand-alone graphene mixers, *i.e.*, mixers with a built-in LO. To this end, the RO shown in Figure 1a was modified by superimposing a radio frequency (RF) signal $v_{rf}(t) = V_{rf} \sin(2\pi f_{RF} t)$ over the dc supply V_{DD} of the decoupling inverter 4 (without affecting the supplies of the other three inverters, Figure S17); hence $v_{DD4}(t) = V_{DD} + v_{rf}(t)$. As the other three inverters forming a ring are not affected by the addition of the RF signal, the alternating current (ac) component of the oscillating voltage at the input of the fourth inverter is also unaltered, which is to a first approximation $v_{in4}(t) \approx V_{in4} \sin(2\pi f_{LO} t)$, where $f_{LO} = f_o$. The RF signal modulates the supply of the fourth inverter and thereby changes its voltage gain. Assuming a linear relationship between A_{v4} and $v_{DD4}(t)$,[12] the voltage gain is $A_{v4}(v_{DD4}) = A_{v4}(V_{DD}) - kv_{rf}$, where k is the proportionality factor ($k \approx 2\ V^{-1}$). The ac component of the output signal is then $v_{out}(t) = A_{v4}v_{in4} = A_{v4}(V_{DD})v_{in4} - kv_{rf}v_{in4}$.

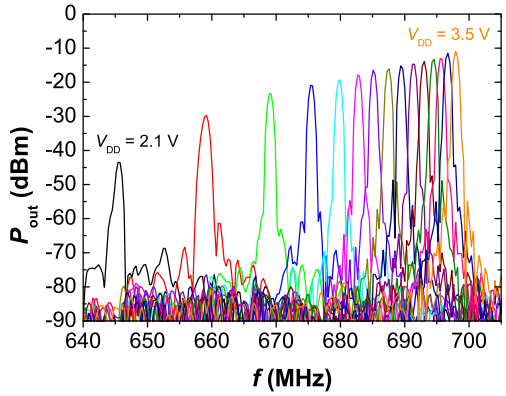

Figure 3. Power spectrum of the output signal measured in a medium-size buffered RO (L = 2 μm and W = 10 μm) at different supply voltages as labeled, and V_{BG} = 89 V. From left to right: V_{DD} = 2.1 to 3.5 V in steps of 0.1 V. At larger V_{DD} the drain conductance increases more slowly, and therefore the oscillation frequency increases more slowly with the increase of V_{DD}. This results in reduced spacing between the maxima in the power spectrum at larger V_{DD}.

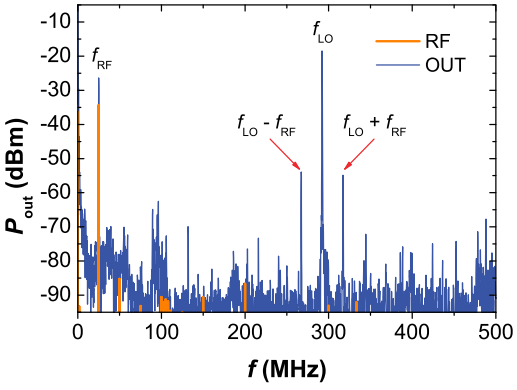

Figure 4. Power spectrum of the input (RF) and output (OUT) signals of the stand-alone graphene mixer at V_{DD} = 2.5 V and V_{BG} = 166 V. The signal frequencies are f_{LO} = 292 MHz and f_{RF} = 25 MHz. Apart from the signals discussed in the main text, the output signal also contains a frequency component at f_{RF}, which comes from the amplification of the RF signal by the inverter 4. The output signal in the time domain is shown in Figure S18.

Figure 4 shows the power spectrum of the output signal in which both terms from the previous expression can be seen. The first term is the signal of the LO at a frequency f_{LO}, whereas the second term is the product of the LO and RF signals $\propto \sin(2\pi f_{RF} t) \sin(2\pi f_{LO} t)$, which gives rise to intermediate frequencies $f_{LO} \pm f_{RF}$. At larger amplitudes of the RF signal nonlinear intermodulation of the RF and LO signals will generate intermediate frequencies $lf_{LO} \pm mf_{RF}$, where l and m are integers (Figure S19). In this case, the circuit will act as a harmonic mixer. The conversion loss obtained from Figure 4 is 19.6 dB at an LO power of −18.5 dBm and RF power of −34.3 dBm, which is better than in early graphene mixers,[26,27] but worse than in recent graphene mixers.[28,29] Also, the isolation between the

mixer ports is insufficient (*e.g.*, the RF port is not isolated from the LO signal). However, both conversion loss and port isolation could be improved with the current technology, as fabricated inverters exhibit voltage gain. By feeding the RF signal through an additional inverter (*i.e.*, an amplifier) the conversion loss could be reduced and the influence of the LO signal at the RF port could be suppressed. In general, conversion loss is not a critical parameter, as low-gain mixers usually exhibit better noise figures and linearity than high-gain mixers. Required signal levels in the former case are often obtained by filtering the output before passing it to an additional low-noise amplifier stage.

There are several figures of merit that should be considered before graphene can be used in digital applications. The absence of a band gap in graphene results in a nonzero off-state drain current, which leads to considerable static power dissipation. The typical static drain current in our small graphene inverters is $I_D/W \approx 270\ \mu A/\mu m$ at $V_{DD} = 2.5$ V, in contrast to much smaller leakage drain current $I_D/W \approx 100$ nA/μm at $V_{DD} = 0.75$ V in 22 nm node high-performance silicon logic transistors.[30] This prohibits the use of graphene in highly integrated low-power digital applications (such as Si CMOS), even though leakage power also exceeds dynamic (switching) power in most state-of-the-art Si logic circuits.[31,32] Lack of a band gap also reduces the voltage swing in graphene inverters, which together with their nonsaturated transfer curves reduces the noise margin (Figure S20). Finally, in order to reach a voltage gain of >1, the gate oxide thickness in graphene FETs must be more aggressively scaled than the gate length and supply voltage, breaking the conventional scaling laws. The present oxide thickness (~4 nm) is only slightly larger than that of contemporary Si FETs, and in both cases further scaling benefits can be obtained only at the expense of other advances (*e.g.*, use of high-*k* oxides, fins, and strain engineering). The only advantage of graphene ROs with respect to Si CMOS ROs is a smaller sensitivity to supply fluctuations; however, this comes as a consequence of the reduced voltage swing. The graphene ROs also exhibit larger phase noise than Si ROs (Figure S21).

Graphene can find applications in EHF digital circuits in which large charge carrier mobility leads to high operating speed, which could be traded off against power dissipation, reduced voltage swing, and circuit complexity.[7,33−35] However, before graphene can be considered as a replacement for InP heterojunction bipolar transistors in EHF applications, further technological advances are needed. The inverter delay in the fabricated ROs with $L = 1\ \mu$m is $\tau \approx 100$ ps, which is similar to that of Si CMOS inverters at the same gate length.[36] This is a consequence of similar *extrinsic* charge carrier mobilities ($\mu \approx 500\ cm^2\ V^{-1}\ s^{-1}$) in these two cases. Such low extrinsic mobility of graphene (compared to its intrinsic mobility, which is much larger than that of Si and InP) is a consequence of a large contact resistance (here ~2 k$\Omega\cdot\mu$m) and scattering from charged impurities in the top and back oxide. Both contact resistance and impurity scattering must be reduced if graphene is to replace InP in future EHF circuits. Higher mobility will also allow lower supply voltages, thus reestablishing conventional scaling laws. However, graphene can immediately find applications in analog electronics. Oscillators are one of the main building blocks of analog electronics,[37] *e.g.*, RF (microwave) electronics is built on voltage amplifiers, oscillators, and mixers.[25,38] Amplifiers[11,12] and mixers[26,27] have already been demonstrated, and the oscillators demonstrated in this work represent the final missing component for the realization of all-graphene microwave circuits. Finally, graphene electronic circuits can be used on transparent and flexible substrates that are inaccessible to conventional semiconductors.

CONCLUSIONS

In summary, we have demonstrated integrated graphene ROs operating at room temperature, under ambient conditions. The ROs were fabricated from wafer-scale CVD monolayer graphene and were composed of inverters exhibiting signal matching and large voltage gain, $|A_v| > 4$. The fabricated ROs oscillate at the highest frequency (1.28 GHz) reported to date in a strictly low-dimensional transistor material, with the voltage swing (as a fraction of supply voltage) exceeding that of conventional InP ECL gates, the fastest logic family. Graphene ROs are more robust to variations in supply voltage compared to conventional ROs and could be used in applications where ultrafast operation is favored over static power dissipation. We also realized the first graphene stand-alone mixers as a simple demonstration of versatility of the fabricated ROs. Oscillation frequency could be increased through further advances, *e.g.*, by reducing the FET channel length, contact resistance, and parasitic capacitances. Even static power dissipation could be reduced by increasing the voltage swing through the use of AB-stacked bilayer graphene[39−42] once such material becomes available at a wafer scale. The fabricated ROs are an important step toward the application of graphene in electronics.

METHODS

Graphene monolayers (Figure S22) were grown by CVD on Cu with a CH_4 precursor and transferred to SiO_2 (300 nm)/Si substrates. Graphene transistors were patterned by e-beam lithography and reactive-ion etching, whereas the contacts were deposited in an e-beam evaporator. Source and drain

contacts consisted of Au (75 nm), and the gate was made of Al/Ti/Au (45/2/13 nm). The back of the Si substrates was metalized and used as a global back-gate, if needed. Top-gates were fabricated by direct evaporation of Al on graphene, which upon exposure to air naturally forms a very thin (~4 nm) AlO_x gate insulator at the interface with graphene.[21] However, because oxidation would also form an insulating layer on the top surface of the gates, they were terminated with a thin layer of Ti/Au during the same evaporation step (Figure 1c). This approach allowed the formation of ohmic contacts between the gates of one stage and the source/drain terminals of another (Figure 1b). Such internal connections between the output of each inverter and the input of the following inverter significantly reduce parasitic capacitances in the circuit and consequently increase the oscillation frequency. However, the presence of a conductive layer on the top surface of the gates prevents self-alignment of the contacts[9,12] and therefore introduces unwanted access resistances, which reduce the voltage gain. In order to preserve the voltage gain, we reduced the source/drain access resistance by contacting the graphene with purely Au contacts, without the use of a Ti or Cr adhesion layer (Figure S23). Thus, despite the lack of perfectly self-aligned contacts, we were nevertheless able to recover a voltage gain of $|A_V| > 4$ (Figure S2), similar to previous work on self-aligned FETs in which a Ti adhesion layer was used below the Au contacts.[9] Typical dc transfer characteristics are shown in Figure S20.

The circuit layout shown in Figure 1b uses two ground and three V_{DD} supply lines instead of single ground and V_{DD} leads used in typical integrated circuits. This circuit layout was chosen for two reasons: First, it eliminated two extra fabrication steps to realize isolation in the overlap regions between the dc lines. Second, the measurements shown in Figure S17 (mixer) and Figure S2c would not be possible with a single V_{DD} line. A complete circuit layout is shown in Figure S24.

A positive voltage at the Dirac point was found in all fabricated FETs, and therefore a positive back-gate voltage was used to shift the Dirac point back to zero, as described in the main text. Although this allows oscillations in samples with arbitrary large initial Dirac voltages, we found that most of the samples that required large back-gate voltages to oscillate (V_{BG} > 100 V) did not exhibit long-term stability in ambient air. This was due to a back-gate hysteresis that was found to shift the Dirac point of the FETs to larger back-gate voltages even after the Dirac point was shifted to zero (Figures S25–S26). Such samples cannot be used in realistic applications, emphasizing the need for low sample doping.[9] The samples shown in the main text exhibited long-term stability (*e.g.*, the medium RO from Figure 2 also oscillated at zero back-gate voltage). That is, the back-gate voltage was needed only for samples that had high levels of unintentional doping, and it was therefore entirely unnecessary in very clean samples.

All measurements were performed at room temperature. ROs that required low (or zero) back-gate voltages were operated in air. ROs that required large back-gate voltages could not achieve long-term stability without reducing their exposure to air. Although this could be achieved under vacuum, this was not attempted as vacuum is not a typical operating environment of electronic devices and was also found to reduce the voltage gain of the inverters.[9] Instead, such ROs were operated in air under N_2 flow. The voltage signals were measured by Agilent Infiniium DSO9064A (bandwidth 600 MHz) and DSO9254A (2.5 GHz) digital storage oscilloscopes, while the RF signal was generated by a Tektronix AFG 3022B function generator. In order to minimize the parasitic capacitive load of the ROs, the outputs were connected to the oscilloscope *via* Agilent N2795A (bandwidth 1 GHz, capacitance 1 pF), N2796A (2 GHz, 1 pF), and 1158A (4 GHz, 0.8 pF) active probes.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Measurements and discussions on top-gate capacitance, dc characteristics of individual FETs and inverters, extensive modeling and simulations of the fabricated ROs, scaling of the oscillation frequency, detuning of the ROs, the highest frequencies and voltage swings of the fabricated ROs, higher harmonics, output bandwidth, influence of the supply voltage on the oscillation frequency, circuit diagram and output signals in the time domain of the standalone graphene mixers, nonlinear intermodulations in the mixers, noise margin, phase noise, Raman spectrum of monolayer graphene, contact resistance, complete circuit layout, back-gating used to shift the Dirac point, and drift of the transfer curves at large back-gate voltages. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Gigahertz Integrated Graphene Ring Oscillators

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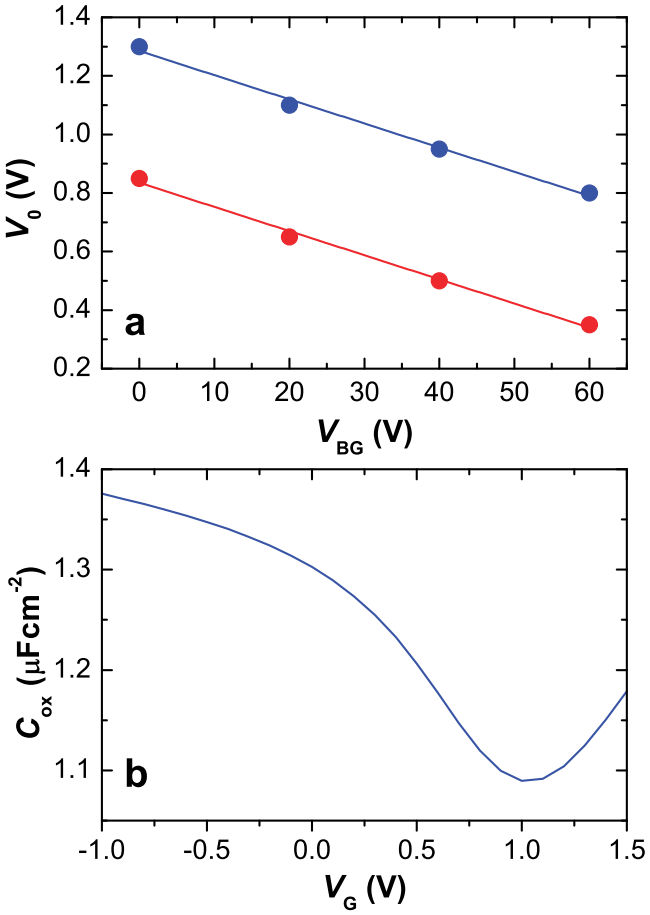

Figure S1: Top-gate capacitance. (a) Position of the Dirac point in the top-gate transfer curve as a function of the back-gate voltage in two different graphene FETs. The ratio of the top-gate to back-gate capacitance per unit area can be determined from the slope of the curve as $C_{\rm ox}/C_{\rm ox,BG} = -dV_{\rm BG}/dV_0 = 121.2$. This gives for the top-gate capacitance per unit area $C_{\rm ox} = 121.2\ C_{\rm ox,BG} = 1.39\ \mu$Fcm^{-2}, where $C_{\rm ox,BG} = \varepsilon_0\varepsilon_{\rm r,SiO_2}/t_{\rm SiO_2} = 11.5$ nFcm^{-2} is the back-gate capacitance per unit area, ε_0 is the vacuum permittivity, and $\varepsilon_{\rm r,SiO_2} = 3.9$ and $t_{\rm SiO_2} = 300$ nm are the relative permittivity and thickness of the back-gate insulator SiO_2, respectively. The top-gate capacitance $C_{\rm G} = LWC_{\rm ox}$ is then $C_{\rm G} = 0.84$ pF (for $L = 3\ \mu$m and $W = 20\ \mu$m), $C_{\rm G} = 0.28$ pF (for $L = 2\ \mu$m and $W = 10\ \mu$m), and $C_{\rm G} = 0.14$ pF (for $L = 1\ \mu$m and $W = 10\ \mu$m). (b) Top-gate capacitance determined from C-V measurements. The measured values are close to $C_{\rm ox} \approx 1.4\ \mu$Fcm^{-2} obtained from the Dirac ratio voltage method.

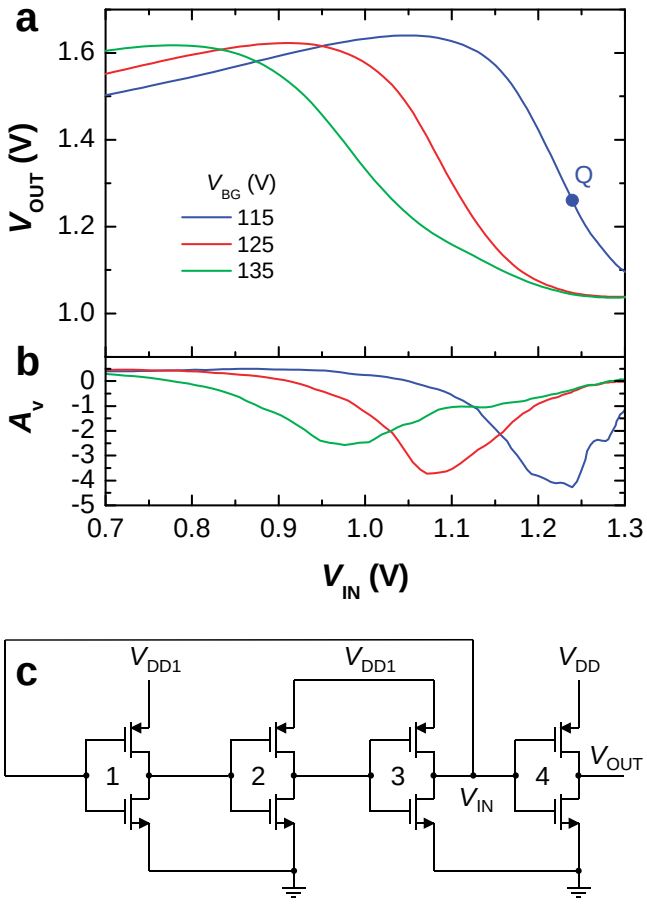

Figure S2: DC characteristics and schematics of a graphene inverter biased with $V_{\mathrm{DD}} = 2.5$ V under different back-gate voltages V_{BG}. (a) Transfer curves of an inverter at different V_{BG}. The highest-gain (threshold) point at which input and output voltages are the same is denoted by Q. (b) The voltage gain A_{v} of the same inverter at different V_{BG}. (c) A schematic diagram of a circuit in which the transfer curves were measured. Although transfer curves are usually measured on the inverter which is not a part of the RO (due to inaccessibility of internal top-gate contacts within a RO),[1,2] we found that it was not necessary to fabricate a separate inverter for this purpose. The top-gate of the output inverter (inverter 4) can be indirectly accessed by separately biasing the previous three inverters with another supply V_{DD1}. Due to circuit symmetry $V_{\mathrm{IN}} \approx V_{\mathrm{DD1}}/2$, i.e., the transfer curves can be measured by varying V_{DD1}.

S1 Large signal model of graphene ROs

S1.1 Steady-state model

Figure S3 shows an equivalent large-signal model of an inverter connected to another inverter (fan-out $N = 1$). In this case, the inverter is loaded only by the gate capacitances of one inverter. The steady-state output voltages and the voltage swing are:

$$V_{\text{on}}^{\infty} = \frac{R_{\text{on}}}{R_{\text{on}} + R_{\text{off}}} V_{\text{DD}}, \tag{1}$$

$$V_{\text{off}}^{\infty} = \frac{R_{\text{off}}}{R_{\text{on}} + R_{\text{off}}} V_{\text{DD}}, \tag{2}$$

$$V_{\text{p-p}} = V_{\text{off}}^{\infty} - V_{\text{on}}^{\infty} = \frac{R_{\text{off}} - R_{\text{on}}}{R_{\text{on}} + R_{\text{off}}} V_{\text{DD}}. \tag{3}$$

The steady-state model assumes that inverters in a RO comprised of n inverters cascaded in a loop will reach the steady-state (described by voltages above) before they are triggered again and forced to change their state. The output voltage of the i-th inverter ($1 \leq i \leq n$) oscillates between V_{on}^{∞} and V_{off}^{∞} (Figure S4) with the time constant

$$\tau_{\text{RC},i} = (R_{\text{on}} \| R_{\text{off}}) N_i (C_{\text{gs}} + C_{\text{A}}) = N_i \tau_{\text{RC}}, \tag{4}$$

$$\tau_{\text{RC}} = (R_{\text{on}} \| R_{\text{off}})(2 + |A_{\text{v}}|) C_{\text{G}}. \tag{5}$$

The only inverter with fan-out $N_i \neq 1$ is the n-th inverter in a buffered RO for which $N_n = 2$. The last expression shows that graphene ROs can oscillate at a frequency approximately twice that of semiconductor ROs (assuming that all other parameters are identical). This is because in graphene FETs $R_{\text{off}} \sim R_{\text{on}}$ and consequently $R_{\text{on}} \| R_{\text{off}} \sim R_{\text{on}}/2$, whereas in semiconductor FETs $R_{\text{off}} \to \infty$ and therefore $R_{\text{on}} \| R_{\text{off}} = R_{\text{on}}$. However, the increase in oscillation frequency is traded off against the lower voltage swing in graphene ROs because $V_{\text{p-p}} < V_{\text{DD}}$.

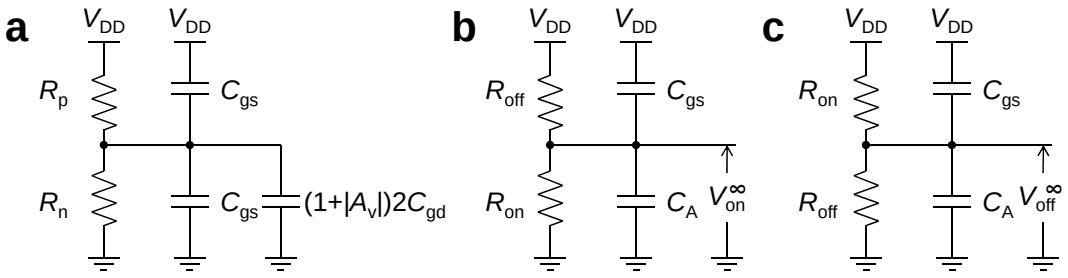

Figure S3: Large signal model of a graphene inverter loaded with another identical inverter. (a) Graphene FETs are represented as resistances R_n and R_p. The model assumes that the inverter is loaded only by the capacitances of the following inverter (by neglecting its own output capacitances; in this way the equivalent load in the case of more loading inverters is simply the load of one inverter multiplied by the fan-out). Apart from the two gate-source capacitances ($C_{\rm gs}$), the inverter is also loaded by two floating gate-drain capacitances ($C_{\rm gd}$) which can be replaced by a grounded Miller capacitance $(1+|A_{\rm v}|)2C_{\rm gd}$. We assumed $C_{\rm gs} = C_{\rm gd} = C_{\rm G}/2$, where $C_{\rm G}$ is the gate-to-channel capacitance determined in Figure S1. Caution should be exercised in interpreting results obtained from this simple model because none of the capacitances used here are in reality independent of the gate voltage.[3] Moreover, capacitance transformation by the Miller theorem is valid only in a linear system in which low-frequency voltage gain $A_{\rm v}$ can be found at the DC (quiescent) operating point. ROs are nonlinear systems which operate in a large signal mode. $|A_{\rm v}| \sim 4$ obtained in Figure S2 is therefore invalid in this case. We assumed $|A_{\rm v}| = 1$ because the voltage swing in ROs is limited by the unity-gain swing. (b) On-state of the inverter. $R_{\rm on}$ and $R_{\rm off}$ are the on-state and off-state resistances, respectively. When the inverter reaches the steady state, the output voltage $V_{\rm on}^{\infty}$ is simply determined from the resistive voltage divider. $C_{\rm A} = C_{\rm gs} + (1+|A_{\rm v}|)2C_{\rm gd} = (5/2)C_{\rm G}$. (c) Off-state of the inverter. The output voltage in the steady state is $V_{\rm off}^{\infty}$.

The rise voltage of the i-th inverter is (Figure S4):

$$v_{{\rm OUT},i}(t) = V_{\rm off}^{\infty} + (V_{\rm on}^{\infty} - V_{\rm off}^{\infty})e^{-t/\tau_{{\rm RC},i}} \quad \text{for} \quad 0 \le t \le \frac{T}{2}. \tag{6}$$

Assuming that the threshold voltage $V_{\rm th}$ is half way between $V_{\rm on}^{\infty}$ and $V_{\rm off}^{\infty}$ the last expression yields the inverter rise delay

$$\tau_i = \tau_{{\rm RC},i} \ln 2 = N_i \tau \tag{7}$$

$$\tau = \tau_{\rm RC} \ln 2. \tag{8}$$

An identical expression is obtained for the inverter fall delay.

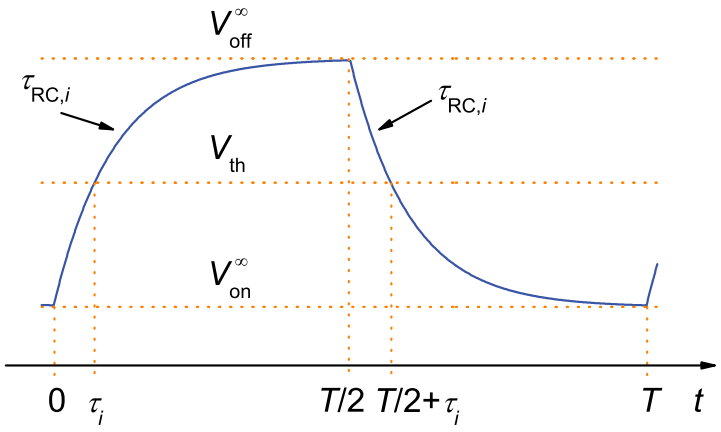

Figure S4: Output signal of an inverter in the steady-state model.

In order to determine $\tau_{\rm RC}$ it is necessary to find $R_{\rm on}$ and $R_{\rm off}$. To a first approximation $R_{\rm off} = R_0$, where R_0 is the resistance at the Dirac point. The expression for $R_{\rm on}$ can be determined from the expression for the voltage swing:

$$R_{\rm on} = \frac{1-p}{1+p} R_{\rm off}, \tag{9}$$

$$R_{\rm on} \| R_{\rm off} = \frac{1-p}{2} R_0, \tag{10}$$

$$p = \frac{V_{\rm p-p}}{V_{\rm DD}}, \tag{11}$$

$$\tau_{\rm RC} = (1-p)(1+\frac{|A_{\rm v}|}{2}) R_0 C_{\rm G}, \tag{12}$$

$$\tau = (1-p)(1+\frac{|A_{\rm v}|}{2}) \ln(2) R_0 C_{\rm G}. \tag{13}$$

The typical voltage swing in an isolated inverter is $p \sim 20\%$,[4] which yields $\tau = 0.83 R_0 C_{\rm G}$. The oscillation frequency is

$$f_{\rm o} = \frac{1}{2\sum_{i=1}^{n} \tau_i} = \frac{1}{2((n-1)\tau + N_n \tau)} = \frac{f_{\rm o,max}}{1+\frac{N_n - 1}{n}}, \tag{14}$$

$$f_{\rm o,max} = \frac{1}{2n\tau}. \tag{15}$$

In an unbuffered RO ($N_n = 1$) the oscillation frequency is $f_{\rm o} = f_{\rm o,max}$ whereas in a buffered

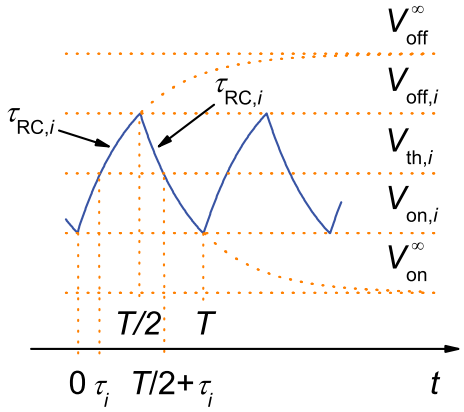

Figure S5: Output signal of an inverter in the transient model.

RO ($N_n = 2$), the oscillation frequency is $f_o = (3/4)f_{o,max}$ for $n = 3$. The numerical values are shown in Table S1 on page 11.

This simple model underestimates the oscillation frequency in the case of ROs with a small number of inverters. In such ROs, an inverter will be triggered before reaching the steady state (because signal propagation through the loop takes less time). For this reason, experimentally measured signals do not have the shape of the signal shown in Figure S4. Assuming that the steady state is reached after three time constants $\tau_{RC,i}$, the condition for reaching the steady state is

$$(n-1)\tau + N_n\tau > 3N_i\tau_{RC} \Rightarrow n > 1 + \frac{3N_i}{\ln(2)} - N_n = \begin{cases} 4.3 & \text{for unbuffered RO} \\ 3.3 & \text{for buffered RO, } i \neq n \\ 7.7 & \text{for buffered RO, } i = n \end{cases} \quad (16)$$

which is not satisfied for any of the inverters in a RO with $n = 3$.

S1.2 Transient model

The transient model assumes that inverters will not reach the steady state before they are triggered again. In this case, the output voltage of an inverter is shown in Figure S5. The

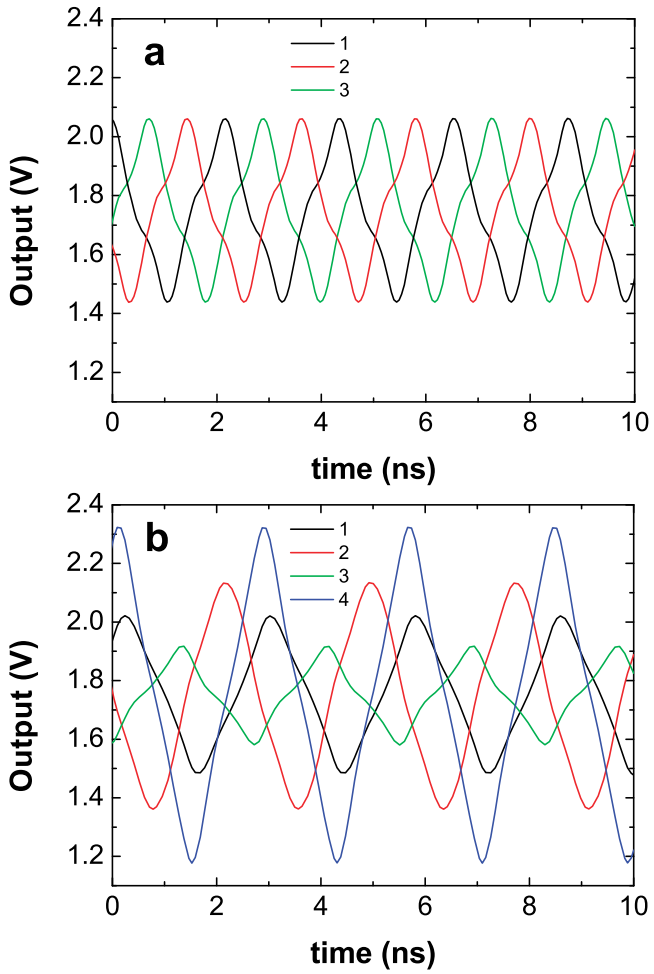

Figure S6: SPICE simulations of large graphene ROs ($L = 3$ μm and $W = 20$ μm) without measurement equipment for $V_{\mathrm{DD}} = 3.5$ V. (a) Output signals of the three inverters in an unbuffered graphene RO. Apart from the phase shift, all three signals are identical due to circuit symmetry. (b) Output signals of the four inverters in a buffered graphene RO. The third inverter has the smallest voltage swing because this inverter has the largest load (i.e., the largest time constant due to the largest fan-out $N_3 = 2$). The output signal is obtained by non-linear amplification of this signal and has the largest voltage swing.

rise voltage is now

$$v_{\mathrm{OUT,i}}(t) = V_{\mathrm{off}}^{\infty} + (V_{\mathrm{on},i} - V_{\mathrm{off}}^{\infty})e^{-t/\tau_{\mathrm{RC},i}} \quad \text{for} \quad 0 \leq t \leq \frac{T}{2}, \tag{17}$$

from which the following expressions can be obtained:

$$V_{\mathrm{th},i} = \frac{V_{\mathrm{on},i} + V_{\mathrm{off},i}}{2} = V_{\mathrm{off}}^{\infty} + (V_{\mathrm{on},i} - V_{\mathrm{off}}^{\infty}) e^{-\tau_i/\tau_{\mathrm{RC},i}}, \tag{18}$$

$$V_{\mathrm{off},i} = V_{\mathrm{off}}^{\infty} + (V_{\mathrm{on},i} - V_{\mathrm{off}}^{\infty}) e^{-T/(2\tau_{\mathrm{RC},i})}. \tag{19}$$

Simple algebraic manipulation of the previous two equations yields

$$1 + e^{-T/(2\tau_{\mathrm{RC},i})} = 2e^{-\tau_i/\tau_{\mathrm{RC},i}}, \tag{20}$$

which leads to the following equations

$$1 + e^{-T/(2\tau_{\mathrm{RC}})} = 2e^{-\tau/\tau_{\mathrm{RC}}},\ \tau_i = \tau \quad \text{if} \quad 1 \le i < n \tag{21}$$

$$1 + e^{-T/(2N_n\tau_{\mathrm{RC}})} = 2e^{-\tau_n/(N_n\tau_{\mathrm{RC}})} \quad \text{if} \quad i = n \tag{22}$$

This yields

$$\frac{T}{2} = (n-1)\tau + \tau_n = (n-1)\tau_{\mathrm{RC}} \ln \frac{2}{1 + e^{-T/(2\tau_{\mathrm{RC}})}} + N_n \tau_{\mathrm{RC}} \ln \frac{2}{1 + e^{-T/(2N_n\tau_{\mathrm{RC}})}}. \tag{23}$$

Substituting

$$x = \frac{T}{2\tau_{\mathrm{RC}}} \tag{24}$$

the last equation transforms into

$$x = (n-1) \ln \frac{2}{1 + e^{-x}} + N_n \ln \frac{2}{1 + e^{-x/N_n}}. \tag{25}$$

Solutions of this equation for $n = 3$ are

$$x = \begin{cases} \ln(2 + \sqrt{5}) & \text{if } N_n = 1 \\ \ln(3 + 2\sqrt{2}) & \text{if } N_n = 2 \end{cases} \tag{26}$$

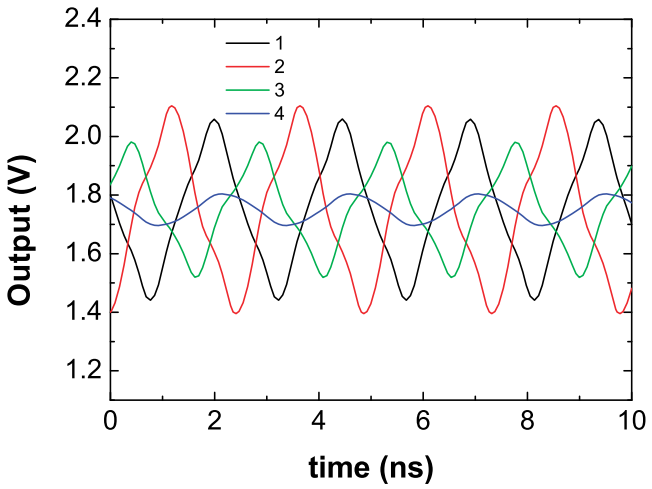

Figure S7: SPICE simulation of a buffered large graphene RO ($L = 3$ μm and $W = 20$ μm) loaded with measurement equipment which introduces an additional load $C_{\mathrm{L}} = 20$ pF on the output inverter. Low-pass filtering by the additional load suppresses the output voltage swing compared to a RO without the additional load (Figure S6b). $V_{\mathrm{DD}} = 3.5$ V.

Therefore in an unbuffered RO ($N_n = 1$)

$$f_{\mathrm{o,max}} = \frac{1}{2\tau_{\mathrm{RC}}x} = \frac{1}{2\ln(2+\sqrt{5})\tau_{\mathrm{RC}}}, \tag{27}$$

$$\tau_i = \tau = \tau_{\mathrm{RC}} \ln\frac{1+\sqrt{5}}{2},\ 1 \le i \le n, \tag{28}$$

which yields $\tau = 0.58 R_0 C_{\mathrm{G}}$. Hence $f_{\mathrm{o,max}} = 451$ MHz (for large ROs, see Table S1), $f_{\mathrm{o,max}} = 893$ MHz (for medium ROs), and $f_{\mathrm{o,max}} = 2.86$ GHz (for small ROs). For the buffered RO ($N_n = 2$):

$$f_{\mathrm{o}} = \frac{1}{2\tau_{\mathrm{RC}}x} = \frac{1}{2\ln(3+2\sqrt{2})\tau_{\mathrm{RC}}} = \frac{\ln(2+\sqrt{5})}{\ln(3+2\sqrt{2})} f_{\mathrm{o,max}}, \tag{29}$$

$$\tau_i = \tau_{\mathrm{RC}} \ln\frac{2+\sqrt{2}}{2},\ 1 \le i < n, \tag{30}$$

$$\tau_n = \tau_{\mathrm{RC}} \ln 2. \tag{31}$$

which yields $f_{\mathrm{o}} = 370$ MHz (for large ROs, compare with the blue signal in Figure 2), $f_{\mathrm{o}} = 731$ MHz (for medium ROs, compare with the green signal in Figure 2), and $f_{\mathrm{o}} = 2.34$ GHz (for small ROs). This model gives a very good description of the fabricated large

Table S1: Parameters of the fabricated ROs and corresponding oscillation frequencies obtained from the steady-state, transient, and SPICE model, and measurements (Figure 2). Values for the Dirac resistance R_0 were measured in actual circuits while the gate capacitance was calculated as $C_G = LWC_{ox} + SC_{ox,BG}/(2(n+1))$ where C_{ox} and $C_{ox,BG}$ are given in Figure S1, S is the total surface area of a RO (e.g., $S \approx 1550$ $(\mu m)^2$ for a small RO; see Figure 1), and $n = 3$. Scaling $f_o \propto 1/L$ is shown in Figure S9. In general, $f_o < f_{o,max} < f_{max} < f_T$ where f_{max} is the maximum oscillation frequency (at which unilateral power gain is equal to one). The actual $f_{o,max}$ for $L = 1$ μm can be estimated to ~ 1.5 GHz, i.e., 1.5 GHz $< f_{max} < f_T$. A less conservative estimate $3f_{o,max} = 4.5$ GHz $< f_{max} < f_T$ stems from the fact that FETs in a 3-inverter RO (fan-out of 1) can switch at a rate of $3f_{o,max}$ while preserving a voltage gain > 1.

RO	L μm	W μm	R_0 Ω	C_G pF	Steady state		Transient		SPICE		Meas.
					$f_{o,max}$ MHz	f_o MHz	$f_{o,max}$ MHz	f_o MHz	$f_{o,max}$ MHz	f_o MHz	f_o MHz
large	3	20	733	0.87	313	235	451	370	457	359	350
medium	2	10	1055	0.31	620	465	893	731	811	648	618
small	1	10	624	0.16	1984	1488	2858	2340	2076	1760	1220

and medium graphene ROs, but it overestimates the oscillation frequency of small ROs. However, this is mostly because the gate capacitance of small ROs is very small and other parasitic capacitances which are not included in this model (e.g., fringe capacitances) cannot be neglected any more.

S1.3 SPICE model

The experimental results were also confirmed by SPICE simulations of the fabricated graphene ROs. We assumed that at low frequencies graphene FETs behave as simple voltage-controlled resistors:[5]

$$I_D = \left(R_{0,in}^{-1} + 2B|V_G - V_0|\right) V_D, \tag{32}$$

where the intrinsic resistance at the Dirac point $R_{0,in}$ and process parameter B are:

$$R_{0,in}^{-1} = \frac{W}{L} R_s^{-1} = G_{0,in}, \tag{33}$$

$$B = \frac{W}{L} \frac{\mu C_{ox}}{2}. \tag{34}$$

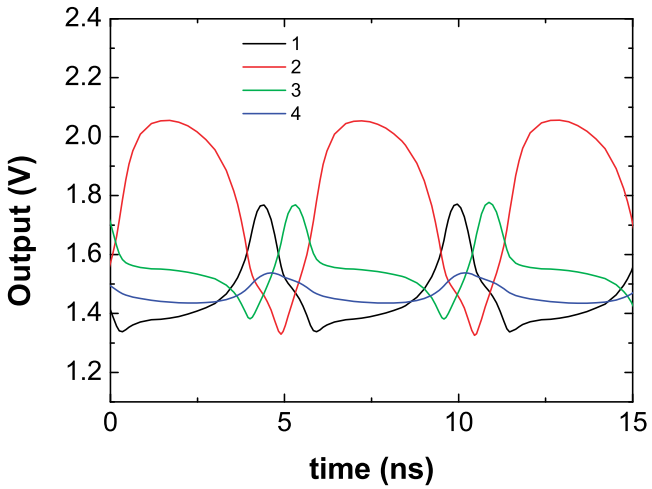

Figure S8: SPICE simulation of a loaded buffered graphene RO shown in Figure S7 in which there is an in-out mismatch $V_0 = 0.29$ V.

Here R_s is the intrinsic sheet resistance of graphene and $\mu \sim 1000$ cm^{2}V^{-1}s^{-1} is the charge carrier mobility (assuming the same mobility for electrons and holes). In order to include contact resistances, we assumed that the total resistance at the Dirac point is

$$R_0 = \frac{L}{W} R_s + \frac{1}{W} R_c, \tag{35}$$

where R_c is the unit width contact resistance. The values in Table S1 give $R_s \approx 4.1$ kΩ/sq and $R_c \approx 2.1$ $k\Omega \cdot \mu$m. The SPICE model was extended to high frequencies by adding capacitances $C_{gs} = C_G/2$ and $C_{gd} = C_G/2$ between the gate and source and the gate and drain, respectively.

Figure S6 shows results of the SPICE simulations of an unbuffered and a buffered large RO. The obtained oscillation frequencies ($f_{o,max} = 457$ MHz for the unbuffered RO and $f_o = 359$ MHz for the buffered RO) are very close to the oscillation frequencies obtained from the transient model. The oscillation frequency of the buffered RO is very close to the measured value of $f_o = 350$ MHz (blue signal in Figure 2).

In the case when the buffer is loaded with the measurement equipment (load $C_L \approx 20$ pF, see Section S3), the output signal will be filtered by increased load, as described in the main text. Figure S7 shows the signals in a loaded buffered RO in which the filtering reduces the

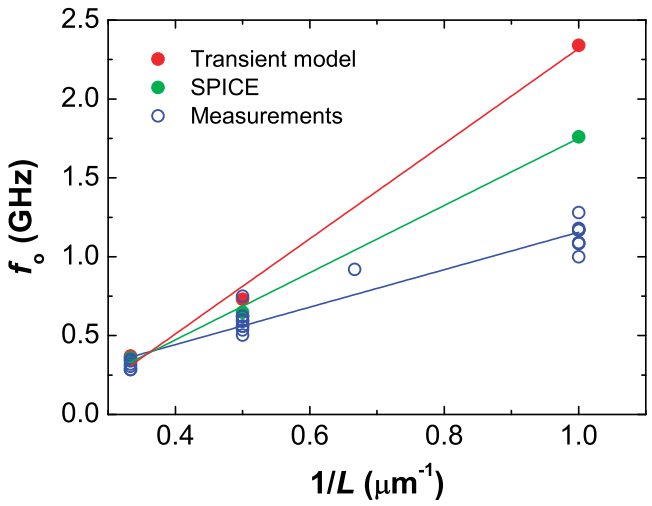

Figure S9: Scaling of the oscillation frequency with $1/L$. The plot shows the values obtained from the transient model (red), SPICE simulations (green), and measurements (blue) performed on 26 ROs (only the highest frequencies for each RO are shown). Apart from the ROs discussed in the text, this plot also includes one RO with $L = 1.5$ μm and $W = 10$ μm.

output amplitude with respect to the RO without measurement load (Figure S6b).

The SPICE model also confirms the appearance of low frequency oscillations in detuned ROs. Figure S8 shows signals in a loaded buffered RO in which there is an in/out mismatch of $V_0 = 0.29$ V. The oscillation frequency is reduced to $f_o = 179$ MHz due to asymmetry. The most extreme case of low-frequency oscillations in a high-frequency RO was observed in a buffered RO shown in Figure S10. When the RO was tuned with a back-gate voltage which avoids in/out mismatch, the oscillation frequency was $f_o = 488$ MHz. However, at a back-gate voltage just 19 V smaller, the oscillation frequency dropped to $f_o = 23.4$ MHz due to detuning.

The simple model (32) can also be used to derive an alternative expression for $R_{on} \| R_{off}$ given by equation (10). The drain conductances of the FETs in a biased inverter ($V_{DD} > 0$) between their Dirac points ($V_{0,n} < V_G < V_{0,p}$) and the total drain conductance are according

to this model (by neglecting the contact resistance, i.e., $R_{0,\mathrm{in}} = R_0 = G_0^{-1}$)

$$G_p = G_0 + 2B(V_{0,p} - V_\mathrm{G}), \tag{36}$$

$$G_n = G_0 + 2B(V_\mathrm{G} - V_{0,p}), \tag{37}$$

$$G_\mathrm{D} = G_p + G_n = 2(G_0 + B(V_{0,p} - V_{0,n})) = 2(G_0 + B\Delta V_0), \tag{38}$$

where $\Delta V_0 = V_{0,p} - V_{0,n} > 0$ is the difference between the Dirac voltages of the FETs in a biased inverter. Finally,

$$R_p \| R_n = \frac{1}{(G_p + G_n)} = \frac{1}{2(G_0 + B\Delta V_0)} = R_\mathrm{on} \| R_\mathrm{off}. \tag{39}$$

S2 Voltage Swing in Graphene ROs

We also investigated unbuffered ROs which do not have the output buffering stage. In this case, the last inverter is loaded both with the measurement equipment and the parasitic capacitance between the output pad and the back-gate, resulting in a total load $C_\mathrm{L} =$ 20 pF (Section S3). Such a large capacitive load significantly increases gate delays and therefore reduces the oscillation frequency. In this case the range of oscillation frequencies was 17 MHz $< f_\mathrm{o} <$ 25 MHz across different ROs.

Unbuffered ROs had a larger voltage swing than that of the buffered ROs described in the main text. This occurs because in both cases signals are filtered by the output capacitive load C_L which limits the output bandwidth to $f_{-3\,\mathrm{dB}} \sim 30$ MHz (Section S3). Filtering more strongly suppresses the signal of the buffered ROs compared to the unbuffered ROs due to the much higher oscillation frequency of the former. The largest voltage swing in unbuffered ROs was 0.57 V, i.e., 16.2% of the supply voltage V_DD (Figure S11), which is close to the 22.4% of V_DD obtained without signal filtering[4] and larger than the swing in the ECL gates.[6] However, in buffered ROs filtering reduces the largest swing to 12.2% V_DD in medium ROs

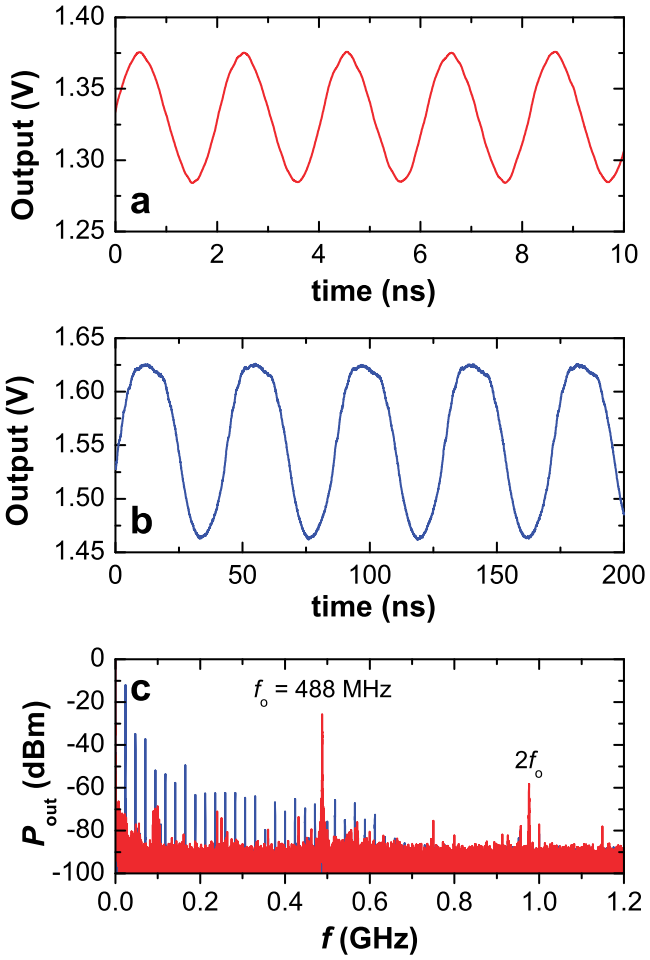

Figure S10: Measured output signals in a buffered RO at $V_{\mathrm{DD}} = 2.5$ V. (a) The RO is tuned (no in/out mismatch) by $V_{\mathrm{BG}} = 140$ V. The oscillation frequency is $f_{\mathrm{o}} = 488$ MHz. (b) The RO is detuned with $V_{\mathrm{BG}} = 121$ V and the oscillation frequency is $f_{\mathrm{o}} = 23.4$ MHz. (c) Power spectra of both signals.

(at 565 MHz, Figure S12) and 5.0% V_{DD} in small ROs (at 1.19 GHz, Figure S12). Filtering also removes higher harmonics from the output signal resulting in featureless (i.e., almost sine wave) signals in case of the buffered ROs. Higher harmonics can easily be observed in unbuffered ROs (Figure S13).

S3 Output bandwidth

The capacitive load introduced to the ROs by the measurement equipment consists of the capacitance of the active probe (≤ 1 pF), the parasitic capacitance of the wire connecting the

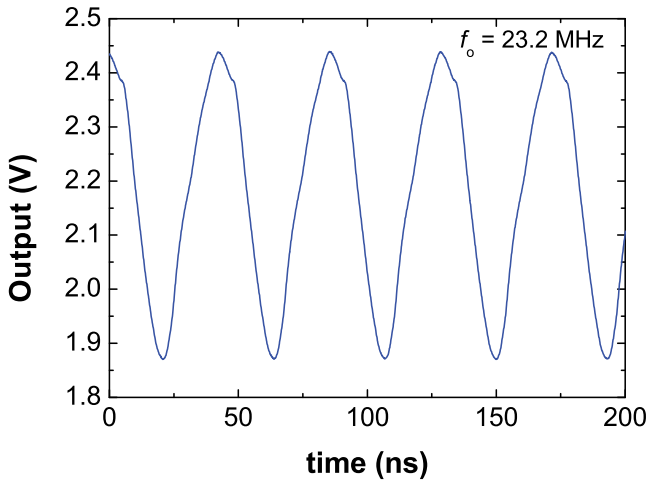

Figure S11: Output signal of an unbuffered RO (without inverter 4 in Figure 1a) at $V_{\mathrm{BG}} = 160$ V and $V_{\mathrm{DD}} = 3.5$ V. The voltage swing is $V_{\mathrm{p-p}} = 0.57$ V.

active probe with the contact probe, the parasitic capacitance of the contact probe, and the parasitic capacitance of the on-chip pad on which the contact probe is placed. In order to find the exact value of this capacitive load, we measured the magnitude of the transfer function $|A(f)|$ of a circuit consisting of a simple graphene resistor in a measurement configuration identical to that of the ROs. Figure S15 shows $|A(f)|$ in the case of a graphene resistor $R = 5.9$ kΩ. From $f_{-3\,\mathrm{dB}} = 1.45$ MHz the capacitive load is $C_{\mathrm{L}} = 1/(2\pi R f_{-3\,\mathrm{dB}}) = 18.6$ pF. Repeated measurements on different resistors yielded 18 pF $\leq C_{\mathrm{L}} \leq$ 22 pF, because of which we assumed $C_{\mathrm{L}} = 20$ pF. This gives for the bandwidth of the last inverter (buffer):

$$f_{-3\,\mathrm{dB}} = \frac{1}{2\pi(R_{\mathrm{on}} \| R_{\mathrm{off}})C_{\mathrm{L}}} = \frac{1}{(1-p)\pi R_0 C_{\mathrm{L}}} = \begin{cases} 27\ \mathrm{MHz} & \text{if } R_0 = 723\ \Omega\ \text{(large RO)} \\ 19\ \mathrm{MHz} & \text{if } R_0 = 1035\ \Omega\ \text{(medium RO)} \\ 32\ \mathrm{MHz} & \text{if } R_0 = 624\ \Omega\ \text{(small RO)} \end{cases} \tag{40}$$

S4 Frequency Dependence on Voltage Supply

In conventional FETs, transient RC effects can be best described by a linear time-invariant drain conductance $G_{\mathrm{D}} = 2B(V_{\mathrm{DD}} - V_{\mathrm{th}})$, where V_{th} is the threshold voltage.[3] This shows

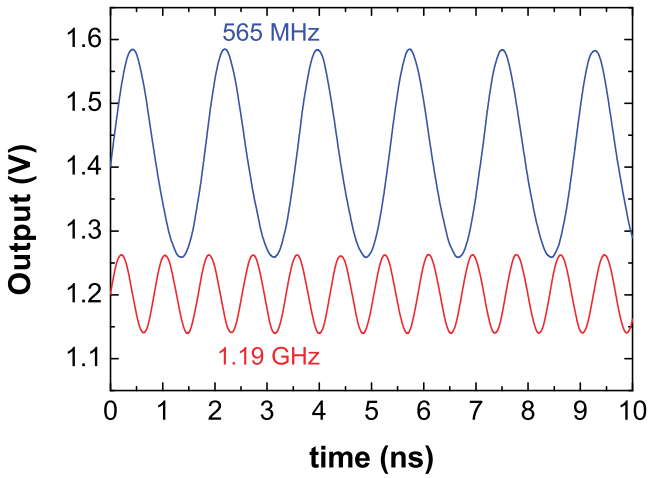

Figure S12: Output signals of small (red; $L = 1$ μm, $W = 10$ μm, $V_{\mathrm{BG}} = 125$ V, and $V_{\mathrm{DD}} = 2.5$ V) and medium (blue; $L = 2$ μm, $W = 10$ μm, $V_{\mathrm{BG}} = 50$ V, and $V_{\mathrm{DD}} = 2.7$ V) buffered ROS with the largest voltage swings. The swing is $V_{\mathrm{p-p}} = 5.0\%$ V_{DD} (small RO) and $V_{\mathrm{p-p}} = 12.2\%$ V_{DD} (medium RO).

that in conventional ROs the oscillation frequency can be reduced to zero provided that the inverters can maintain the gain required to sustain oscillations. However, in graphene ROs $G_{\mathrm{D}} \approx 2(G_0 + B\Delta V_0)$, i.e., there is a minimum non-zero oscillation frequency defined by the total Dirac conductance $2G_0$ (at $\Delta V_0 = 0$). At small Dirac voltage splits ΔV_0 the oscillation frequency becomes almost constant as $G_0 \gg B\Delta V_0$. Moreover, while in conventional ROs the change of frequency is $\partial f_{\mathrm{o}}/\partial V_{\mathrm{DD}} \propto 2B$, in graphene ROs this change is $\partial f_{\mathrm{o}}/\partial V_{\mathrm{DD}} \propto 2B\partial\Delta V_0/\partial V_{\mathrm{DD}}$, which for the same process parameter B is considerably smaller than $2B$. For the RO shown in Figure 3, the change of the oscillation frequency with supply voltage is $\partial f_{\mathrm{o}}/\partial V_{\mathrm{DD}} < 137$ MHz/V $\approx 21\% f_{\mathrm{o}}$/V (Figure S16) or $\sim 5.6\% f_{\mathrm{o}}$/V on average.

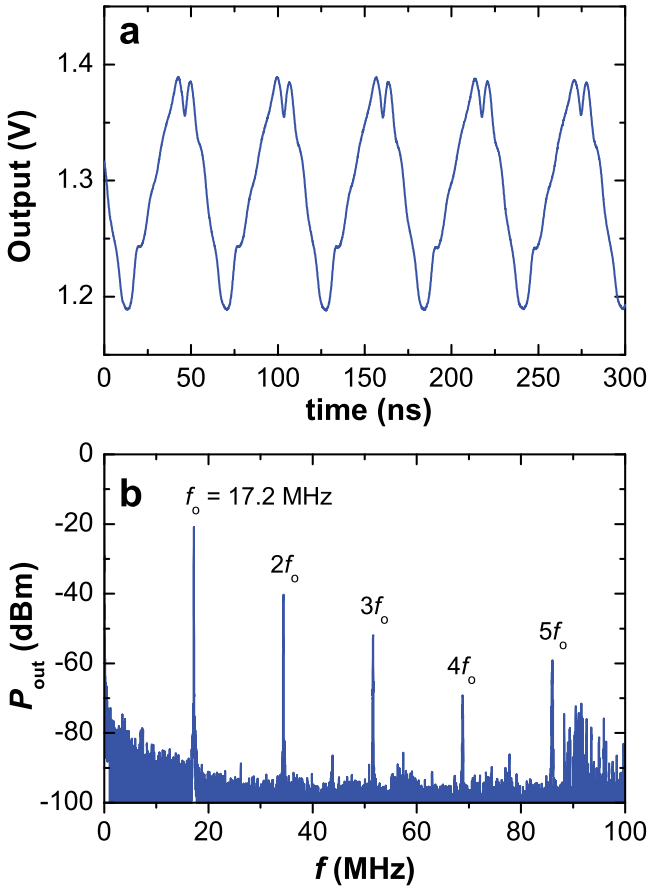

Figure S13: Output signal of an unbuffered RO at $V_{BG} = 6.2$ V and $V_{DD} = 2.5$ V. (a) The output signal in the time domain. (b) The power spectrum of the output signal.

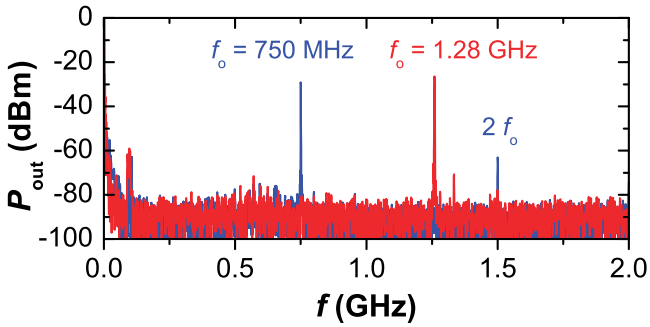

Figure S14: Power spectra of the highest frequency output signals in small (red; $L = 1$ μm, $W = 10$ μm) and medium (blue; $L = 2$ μm, $W = 10$ μm) buffered ROS.

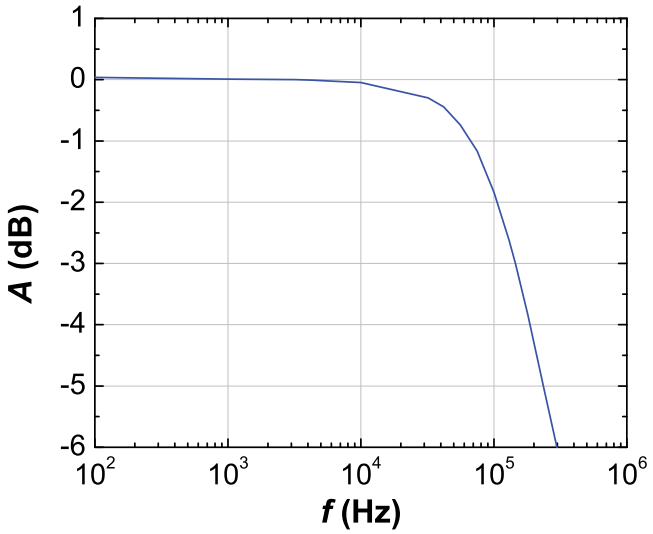

Figure S15: The magnitude of the transfer function $|A(f)|$ in a simple circuit comprised of a known resistor $R = 5.9$ kΩ and unknown capacitance C_{L}. The capacitance can be determined from the bandwidth.

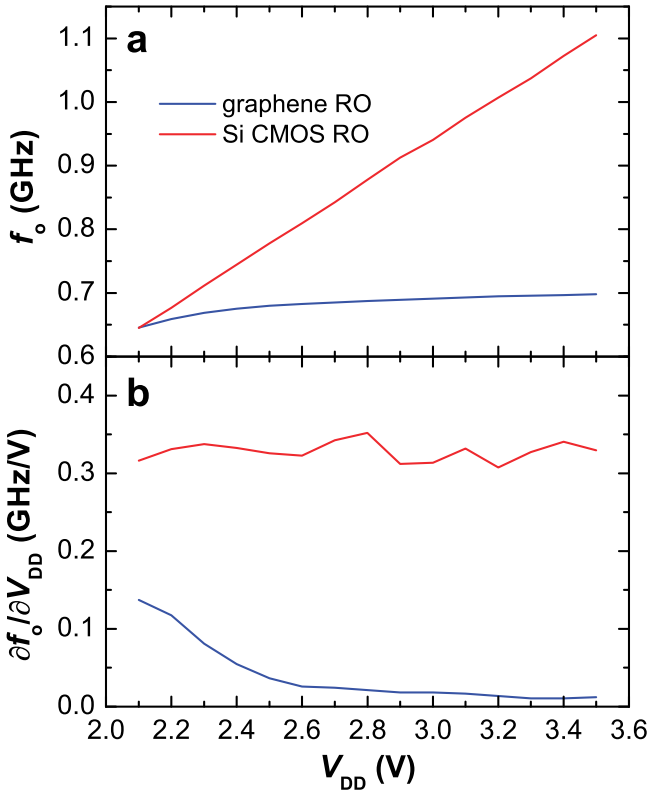

Figure S16: Influence of the supply voltage V_{DD} on the oscillation frequency f_{o} in the RO from Figure 3 and in a Si CMOS RO. (a) Oscillation frequency as a function of the supply voltage. (b) Change of the oscillation frequency $\partial f_{\mathrm{o}}/\partial V_{\mathrm{DD}}$ as a function of V_{DD}. Si CMOS data were obtained from SPICE simulations. MOSFETs parameters ($t_{\mathrm{ox}} = 10$ nm, $L = 2.398$ μm, and $W = 10$ μm) were chosen to obtain the same oscillation frequency at $V_{\mathrm{DD}} = 2.1$ V and $C_{\mathrm{L}} = 20$ pF as in the measured graphene RO.

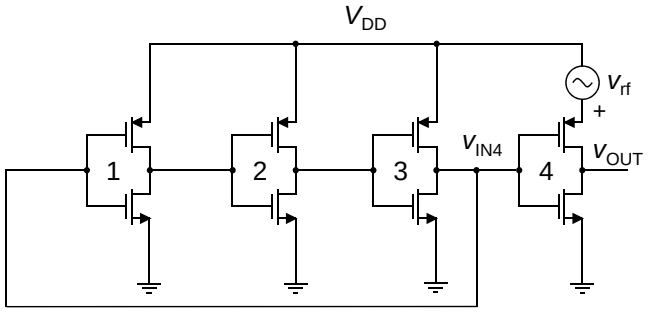

Figure S17: A circuit diagram of a stand-alone graphene mixer. The AC component $v_{\mathrm{out}}(t)$ of the output signal $v_{\mathrm{OUT}}(t)$ contains intermediate frequency components at $f_{\mathrm{LO}} \pm f_{\mathrm{RF}}$ obtained by mixing $v_{\mathrm{rf}}(t)$ with the AC component $v_{\mathrm{in4}}(t)$ of the oscillating signal $v_{\mathrm{IN4}}(t)$.

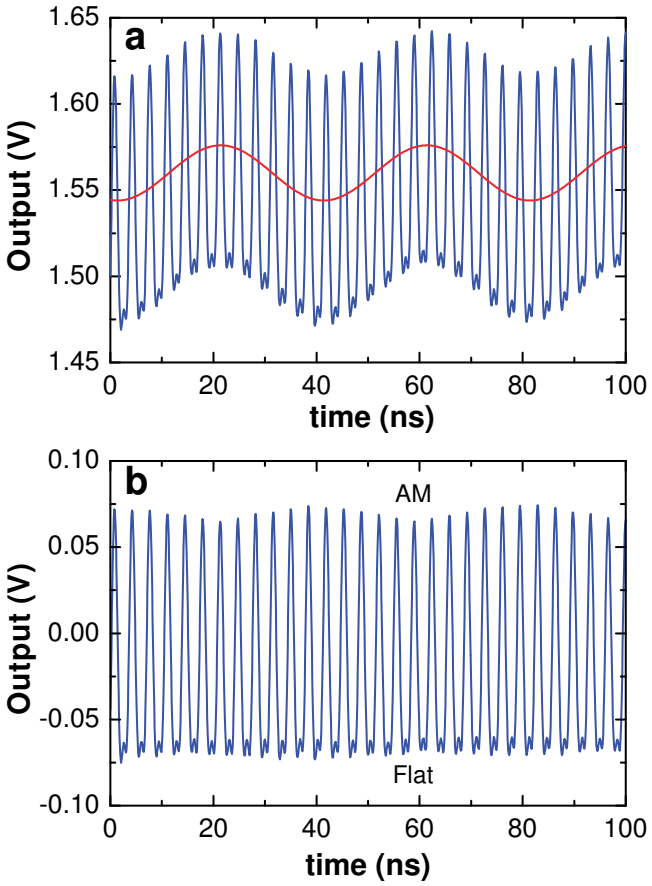

Figure S18: Output signal of a stand-alone graphene mixer in the time domain whose power spectrum is shown in Figure 4. (a) The output signal (blue) and its local average value (red) which is modulated by the RF signal. The average value is a signal at a frequency $f_{\mathrm{RF}} = 25$ MHz and is also visible in the spectrum shown in Figure 4. (b) The output signal after subtracting the modulated average value. The RF signal also modulates the upper envelope of the signal thus performing amplitude modulation (AM). The sidebands at $f_{\mathrm{LO}} \pm f_{\mathrm{RF}}$ shown in Figure 4 are typical of AM signals.

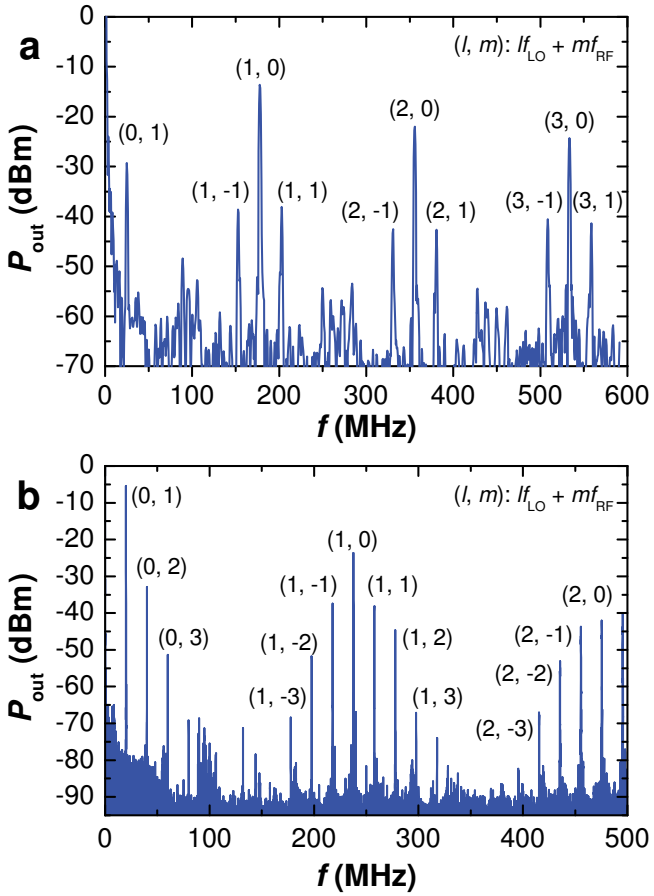

Figure S19: Examples of nonlinear intermodulations $lf_{\mathrm{LO}} \pm mf_{\mathrm{RF}}$ in a stand-alone graphene mixer at larger amplitudes of the RF signal. (a) Intermodulation in which $|m| \leq 1$. (b) Intermodulation in which $|m| \geq 1$. In this case also higher harmonics of the RF signal are visible ($l = 0$, $m > 1$).

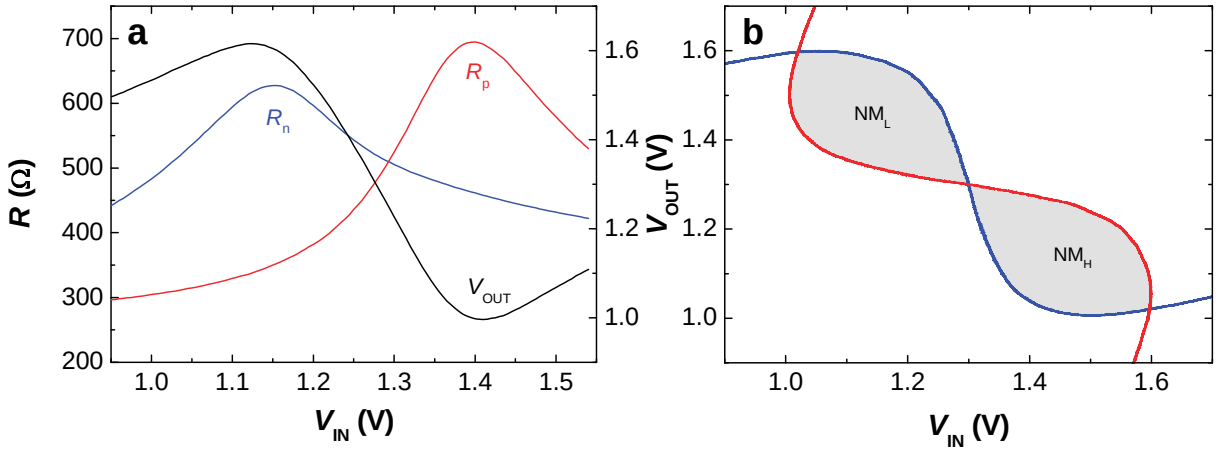

Figure S20: DC transfer characteristics of two different graphene inverters at $V_{\mathrm{DD}} = 2.5$ V. (a) Resistances of typical small FETs ($L = 1$ μm) in an inverter and corresponding transfer curve of the inverter. Fabricated FETs exhibit on/off ~ 2.5. Complementary operation is obtained between the Dirac points of the two FETs. (b) Transfer curve of a graphene inverter (blue) and its mirrored reflection (red). The shaded areas indicate noise margins at low ($\mathrm{NM_L}$) and high ($\mathrm{NM_H}$) input voltages. Non-saturated transfer characteristics of graphene inverters lead to slightly reduced noise margins at the extremes of the input voltage.

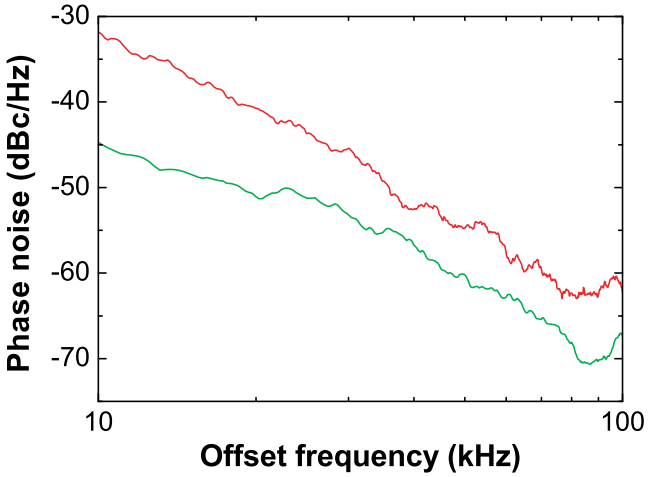

Figure S21: Phase noise measured in two different graphene ROs. The fabricated ROs exhibit larger phase noise than state-of-the-art ROs, which typically present a phase noise < 100 dBc/Hz at an offset frequency of 100 kHz.

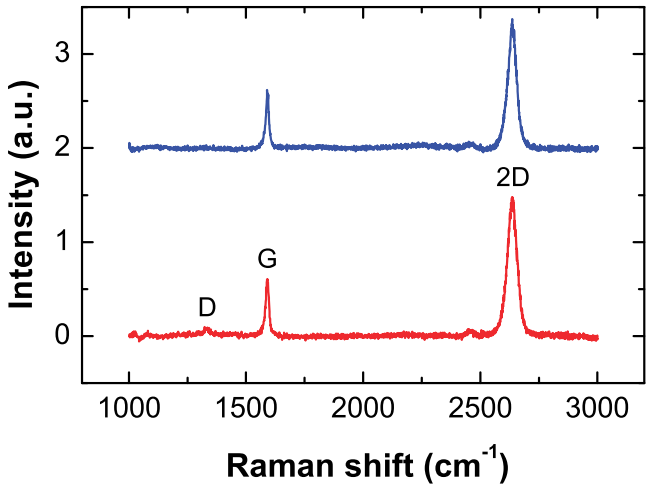

Figure S22: Raman spectra of typical graphene films used in this study. The G/2D peak ratio suggests the presence of primarily monolayer graphene, while the small integrated D/G ratio (< 0.15) implies relatively good quality of graphene grown by chemical vapor deposition (CVD).[7]

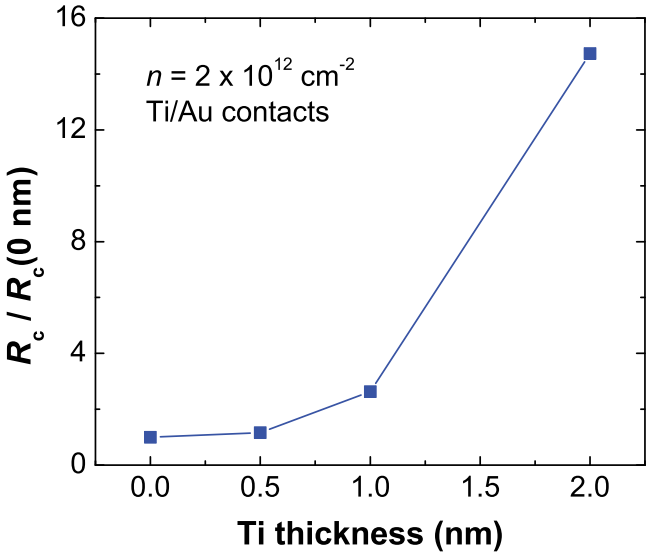

Figure S23: Dependence of the contact resistance R_c on the thickness of the Ti adhesion layer. The resistance is normalized to the resistance at zero thickness.

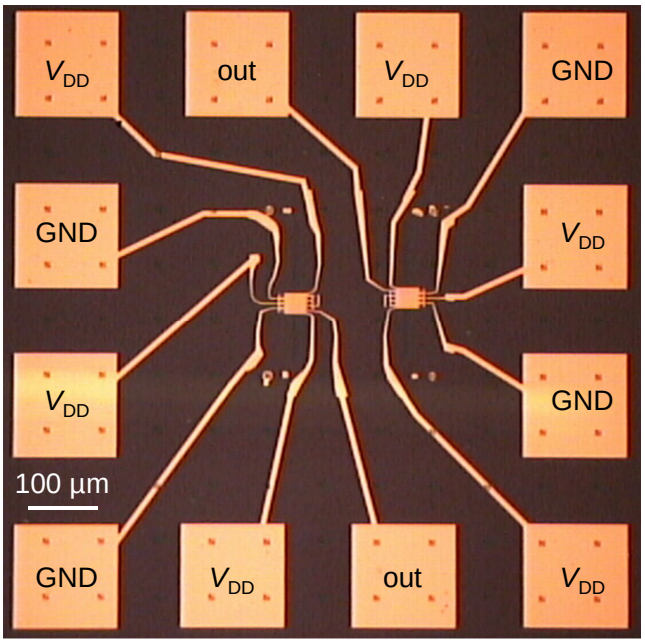

Figure S24: An optical image showing a complete circuit layout of two small ROs. The RO on the left has the same orientation as the RO shown in Figure 1b. The RO on the right is mirrored.

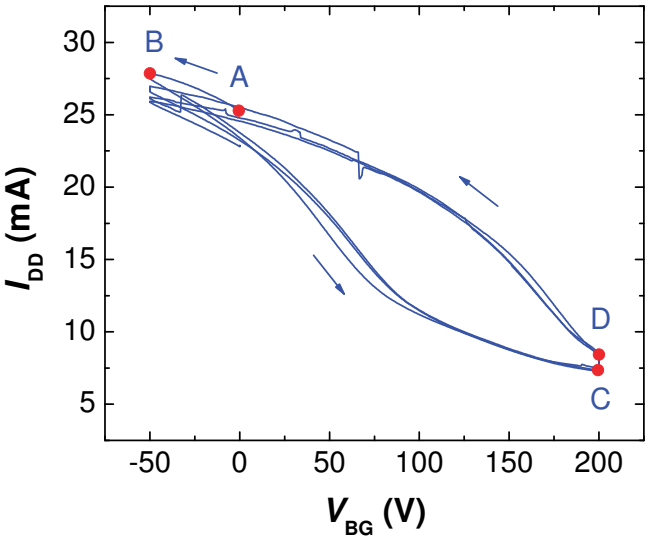

Figure S25: The total current (sum of the currents of all four inverters) as a function of the back-gate voltage in a RO oscillating at $V_{\mathrm{BG}} = 200$ V. The measurement starts at point A ($V_{\mathrm{BG}} = 0$ V). The back-gate voltage is first swept to point B ($V_{\mathrm{BG}} = -50$ V) and then to point C ($V_{\mathrm{BG}} = 200$ V) where oscillations start. During oscillations the back-gate voltage is kept constant, but the total current increases (to point D) detuning the oscillator (because the Dirac voltages increase, see Figure S26). When point D is reached the oscillations are lost and it is necessary to repeat the whole cycle D→B→C to restore the oscillations (three full cycles are shown).

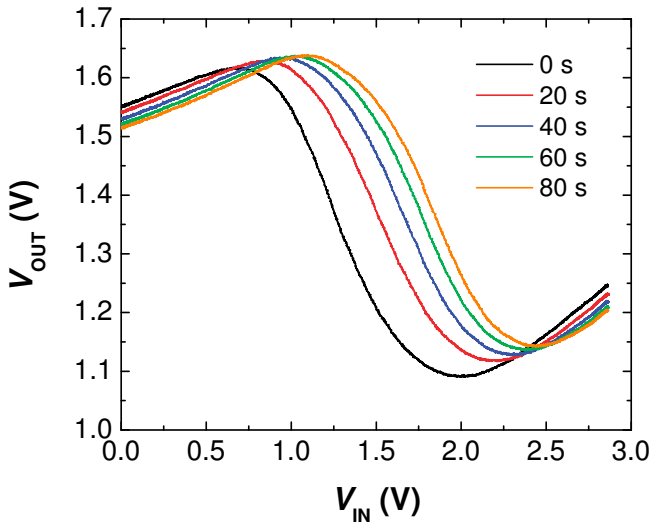

Figure S26: Drift of the transfer curves of a graphene inverter with time at $V_{BG} = 160$ V and $V_{DD} = 2.5$ V. After the first curve (black; 0 s) was measured, subsequent curves were measured at 20 s intervals. The drift is a consequence of the drift of the Dirac point to larger gate voltages, which is more prominent at large back-gate voltages. The drift detunes the RO by introducing in/out mismatch, which stops the RO from oscillating after some time. The oscillations can be restored by further increasing the back-gate voltage or by cycling back the back-gate voltage to the initial state (as described in Figure S25). The former method is of limited use as the drift cannot be stopped and consequently the back-gate voltage would soon reach the oxide breakdown voltage.

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