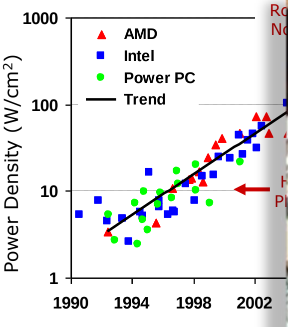
Power Dissipation in Nanoscale CMOS and Carbon Nanotubes

Eric Pop

Dept. of Electrical & Computer Engineering
http://poplab.ece.uiuc.edu

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

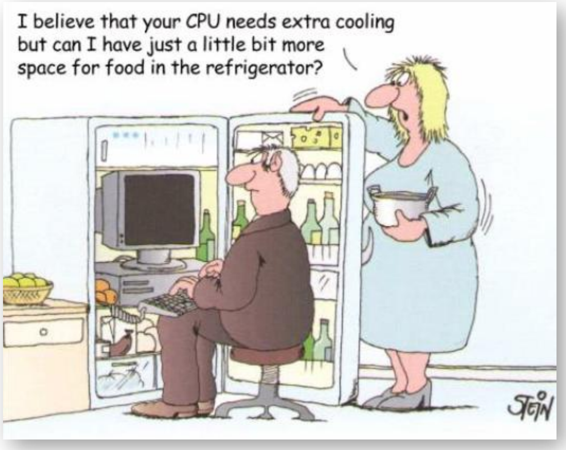
Power and Heat: The *Big* Picture



Sun surface? 6000 W

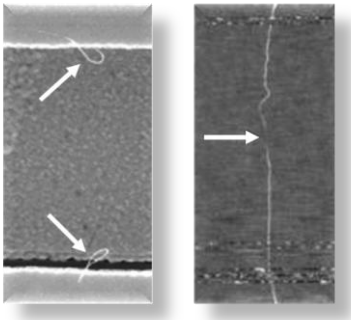
http://phys.ncku.edu.tw/~htsu/humor/fry_egg.html

Thermal Management Challenges



- IBM S/390 refrige
- Grid computing: p

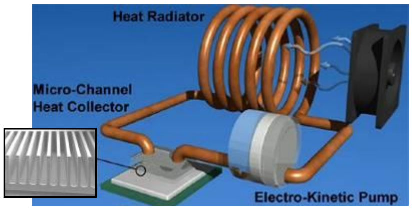
Power and Heat: The *Tiny* Picture

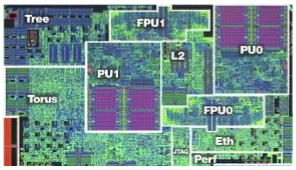


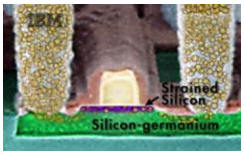
Suspended **On substrate**

Carbon nanotubes *burn* at high enough applied voltage
(they also emit light when they get this hot)

Power, Thermal Management Methods



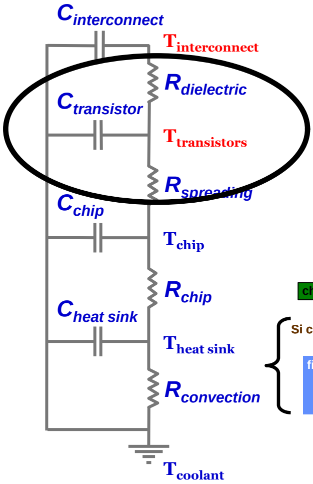




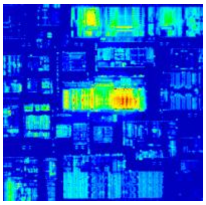
Is there a bottom-up approach?

From the device and materials level?

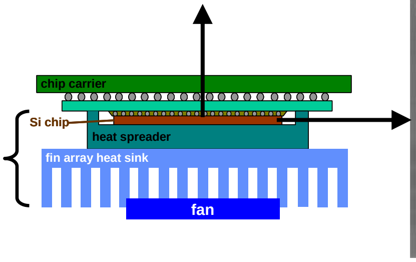
Chip-Level Thermal Network



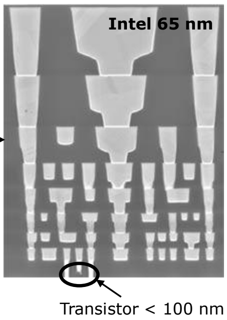
Intel Itanium



Top view
Hottest spots > 300 W/cm²

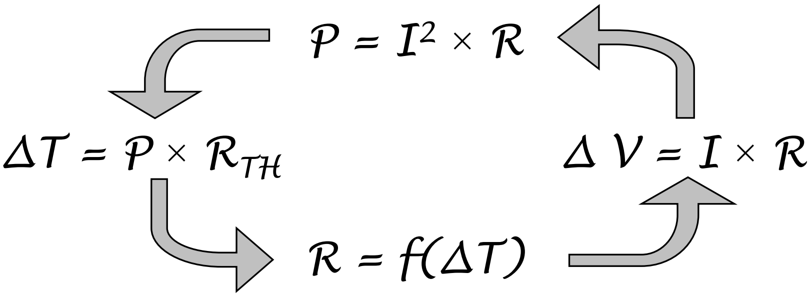


Cross-section
8 metal levels + ILD



Transistor < 100 nm

Thermal and Electrical Resistance



$$P = I^2 \times R$$

$$\Delta T = P \times R_{TH}$$

$$\Delta V = I \times R$$

$$R = f(\Delta T)$$

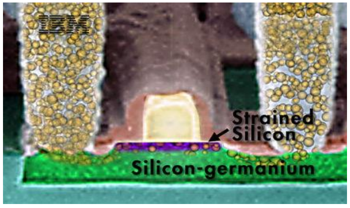
Fourier's Law (1822)

Ohm's Law (1827)

Device-Level Thermal Challenges

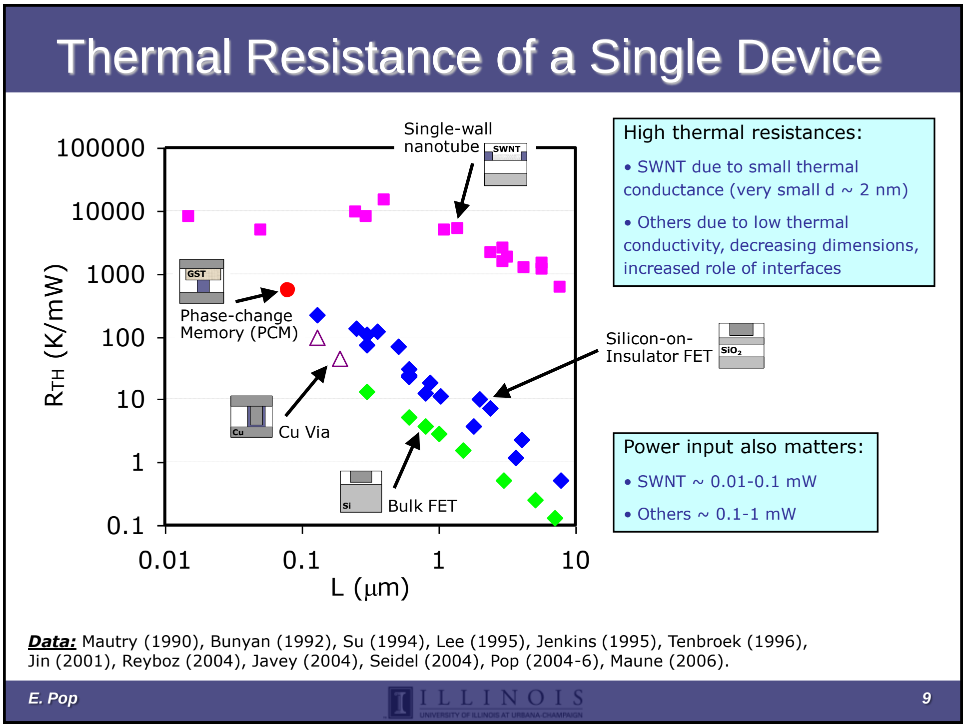
- Small geometry
  - High power density (device-level hot spot)
  - Higher surface-to-volume ratio, i.e. higher role of thermal interfaces between materials
- Lower thermal conductivity
- Lowering power (but can it ever be low enough?!)
- Device-level thermal design (phonon engineering)

Device Level:
Confined Geometries, Novel Materials



Material	*k (W/m/K)*
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO_2	1.4

Source: E. Pop (*Proc. IEEE* 2006)



Thermal Resistance of a Single Device

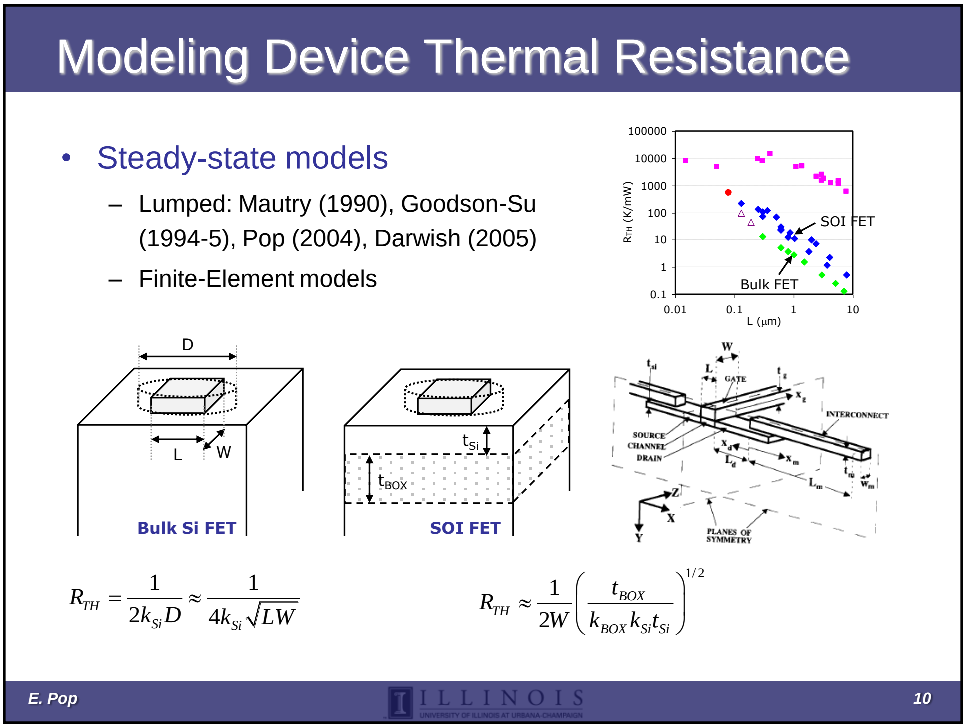
High thermal resistances:

- SWNT due to small thermal conductance (very small d ~ 2 nm)
- Others due to low thermal conductivity, decreasing dimensions, increased role of interfaces

Power input also matters:

- SWNT ~ 0.01-0.1 mW
- Others ~ 0.1-1 mW

Data: Mautry (1990), Bunyan (1992), Su (1994), Lee (1995), Jenkins (1995), Tenbroek (1996), Jin (2001), Reyboz (2004), Javey (2004), Seidel (2004), Pop (2004-6), Maune (2006).



Modeling Device Thermal Resistance

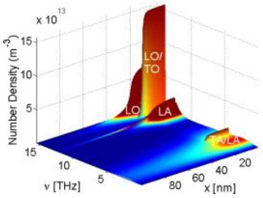
- Steady-state models
  - Lumped: Mautry (1990), Goodson-Su (1994-5), Pop (2004), Darwish (2005)
  - Finite-Element models

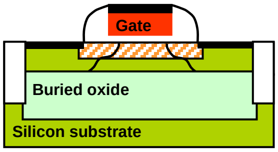
$$R_{TH} = \frac{1}{2k_{Si}D} \approx \frac{1}{4k_{Si}\sqrt{LW}}$$

$$R_{TH} \approx \frac{1}{2W}\left(\frac{t_{BOX}}{k_{BOX}k_{Si}t_{Si}}\right)^{1/2}$$

A More Detailed Look

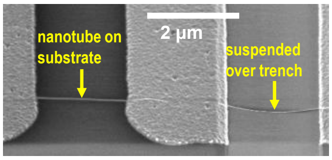
1. **Monte Carlo heat generation in bulk and strained silicon**



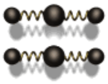


2. **Self-heating in thin-body SOI and GOI devices**

3. **Self-heating and lessons from carbon nanotubes**



Quick Recap of Phonons



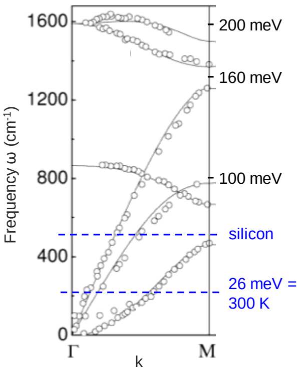
CO_2 molecule vibrations

transverse small k

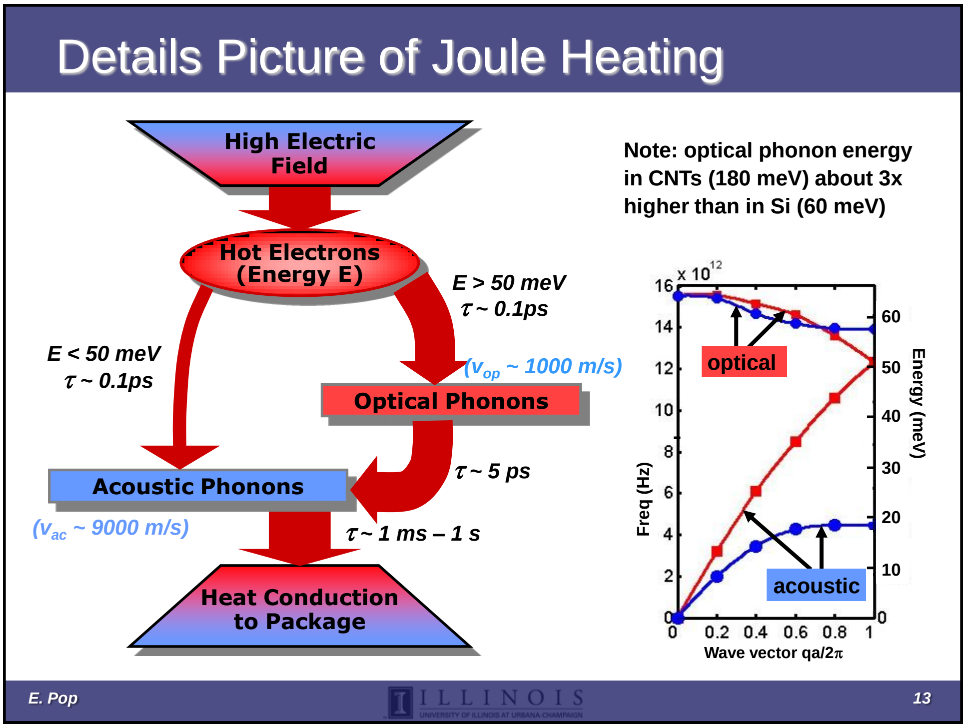
transverse max k=2π/a

$$\mathbf{u}(\mathbf{r},t)=\mathbf{A}\exp[i(\mathbf{k}\cdot\mathbf{r}-i\omega t)]$$

Graphene Phonons [100]



- Phonons = lattice vibration waves
- Phonons are responsible for heat transport in semiconductors
- “Hot phonons” = highly occupied modes above room temperature



Details Picture of Joule Heating

High Electric Field

Hot Electrons (Energy E)

$E > 50$ meV
$\tau \sim 0.1$ps

$E < 50$ meV
$\tau \sim 0.1$ps

($v_{op} \sim 1000$ m/s)

Optical Phonons

$\tau \sim 5$ ps

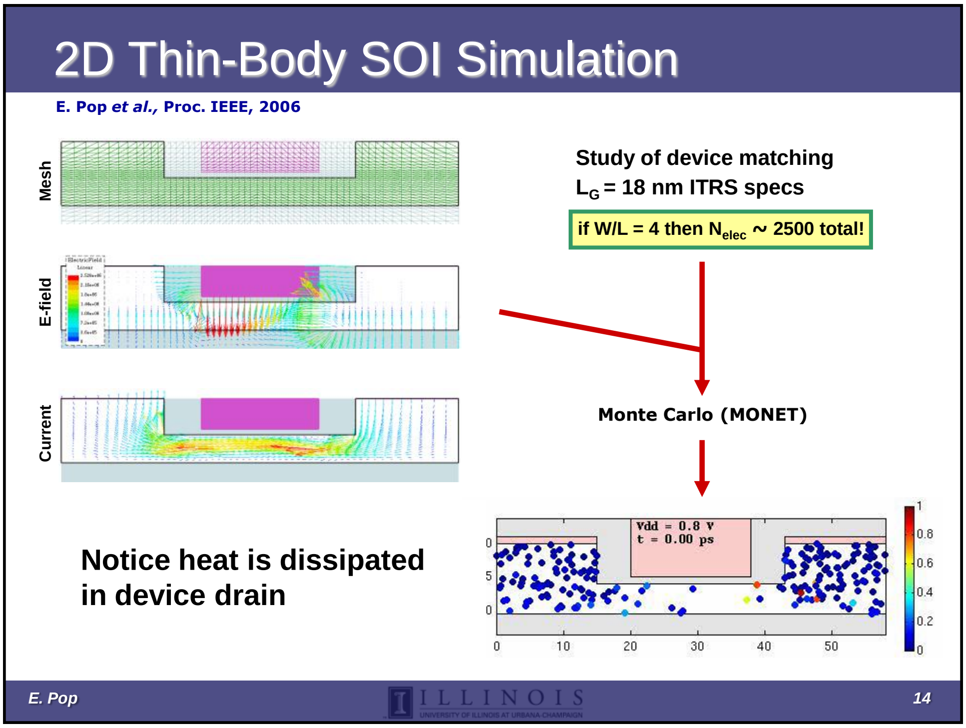
Acoustic Phonons

($v_{ac} \sim 9000$ m/s)

$\tau \sim 1$ ms – 1 s

Heat Conduction to Package

Note: optical phonon energy in CNTs (180 meV) about 3x higher than in Si (60 meV)



2D Thin-Body SOI Simulation

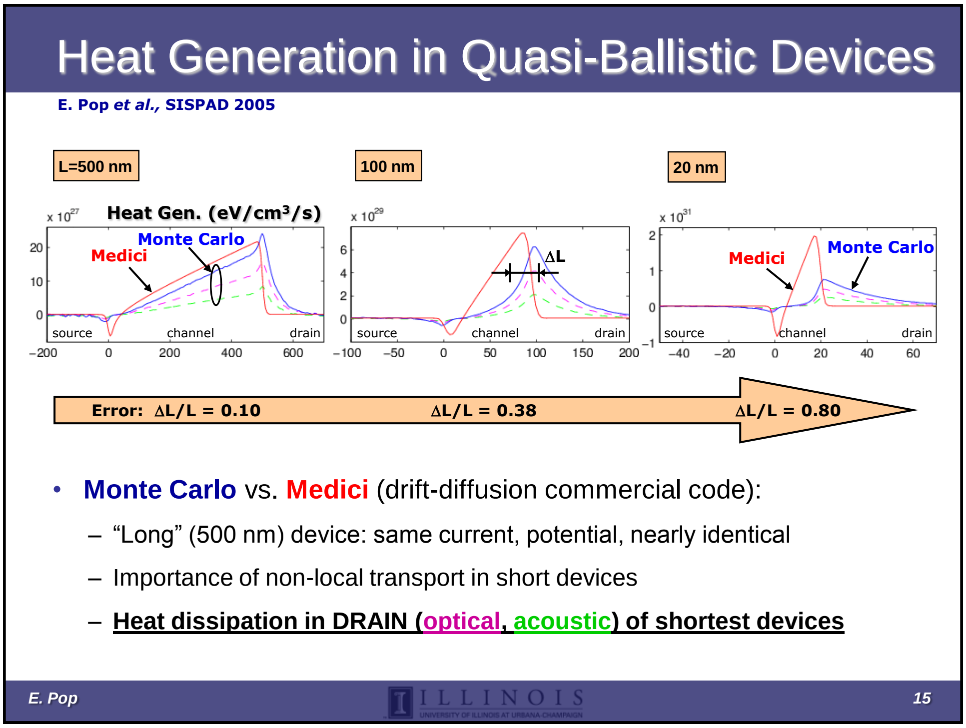
E. Pop *et al.*, Proc. IEEE, 2006

Study of device matching
L_G = 18 nm ITRS specs

if W/L = 4 then N_{elec} ~ 2500 total!

Monte Carlo (MONET)

Notice heat is dissipated in device drain

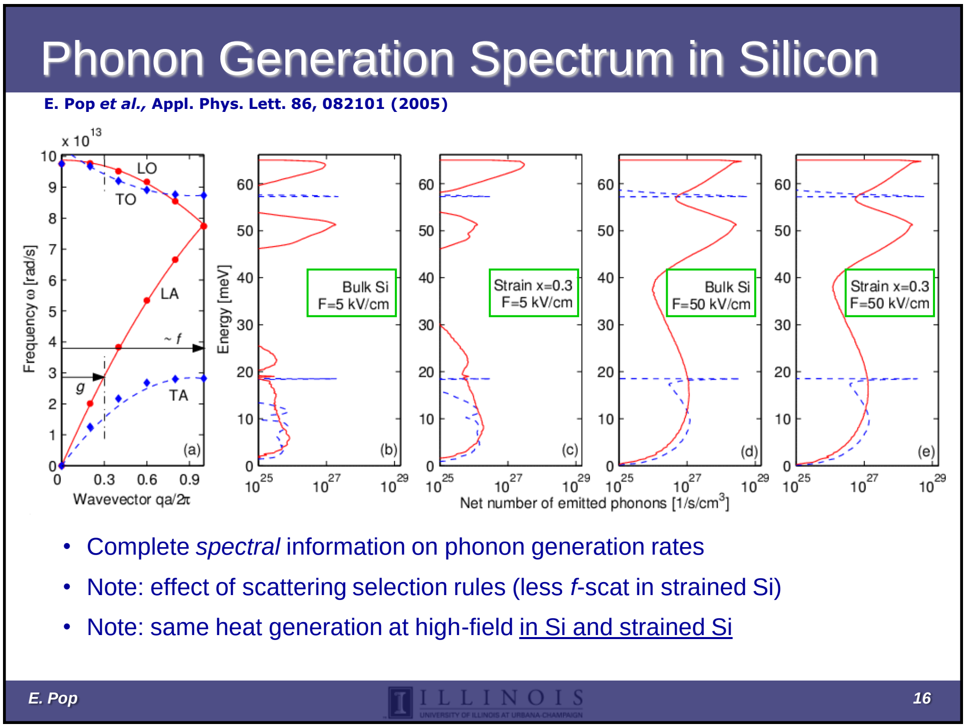


Heat Generation in Quasi-Ballistic Devices

E. Pop *et al.*, SISPAD 2005

Error: ΔL/L = 0.10 **ΔL/L = 0.38** **ΔL/L = 0.80**

- **Monte Carlo** vs. **Medici** (drift-diffusion commercial code):
  - "Long" (500 nm) device: same current, potential, nearly identical
  - Importance of non-local transport in short devices
  - **Heat dissipation in DRAIN (optical, acoustic) of shortest devices**

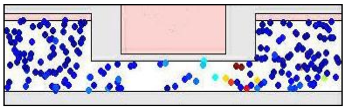


Phonon Generation Spectrum in Silicon

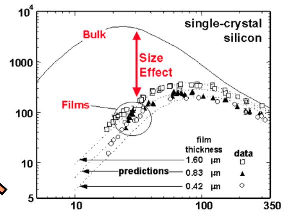
E. Pop *et al.*, Appl. Phys. Lett. 86, 082101 (2005)

- Complete *spectral* information on phonon generation rates
- Note: effect of scattering selection rules (less *f*-scat in strained Si)
- Note: same heat generation at high-field in Si and strained Si

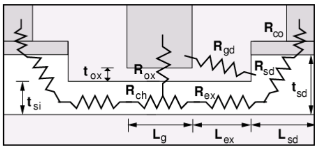
What About Device Design?



Monte Carlo Analysis



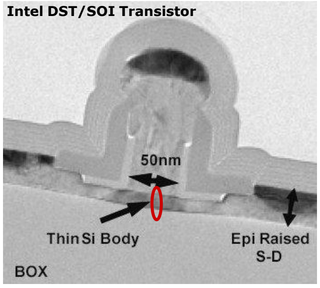
Thermal Conductivity

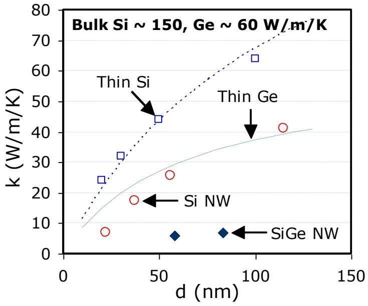


Design and Scaling

Thin Film Thermal Conductivity

E. Pop *et al.*, Proc. IEDM 2003-2004

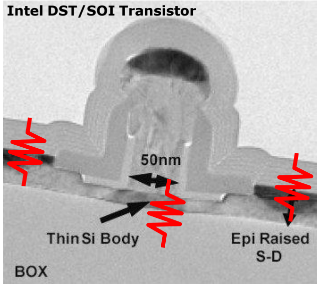


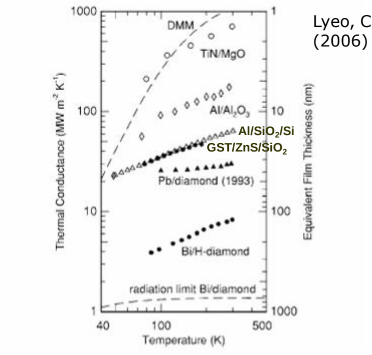


- Phonon boundary scattering and confinement
- Strong *decrease* in thin film or nanowire thermal conductivity (*k*), up to 10-100x lower than bulk
- How does this affect nanometer scale devices?

Boundary Thermal Resistance

E. Pop *et al.*, Proc. IEEE (2006)



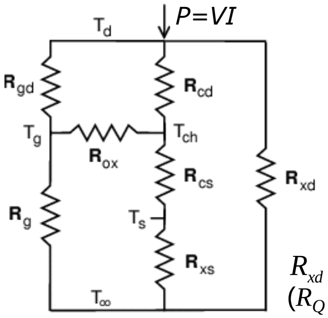


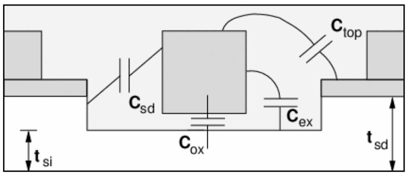
Lyeo, Cahill (2006)

- Thermal interface resistance at solid-solid material interfaces
- Caused by phonon dispersion mismatch b/w materials (~Cv/4), electron-phonon energy conversion at boundary, roughness at boundary
- Approximately equivalent to ~10-100 nm additional SiO_2

Self-Consistent Electro-Thermal Model

E. Pop *et al.*, Proc. IEDM 2004

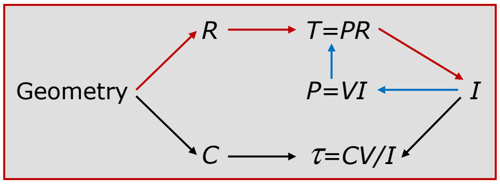




$$C_{ex} = 2\beta\varepsilon_{sw}\ln\left(1 + L_{ex}/t_{ox}\right)/\pi$$

$$R_{xd} = R_{ex} \pm R_Q + R_{sd} + R_{co}$$

(R_Q due to heat source position)


Geometry

R

$T=PR$

$P=VI$

I

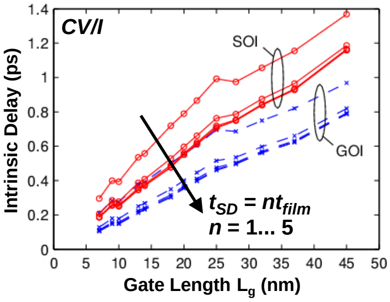
C

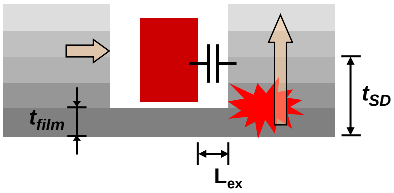
$\tau=CV/I$

$$I \sim \overset{\overset{T^{-1.4}}{\downarrow}}{\mu} \times \left(V_{dd} - \underset{\underset{-0.7\text{ mV/K}}{\uparrow}}{V_t}\right)^n$$

SOI/GOI Device Design Optimization

E. Pop *et al.*, Proc. IEDM 2004

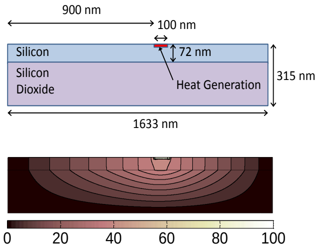


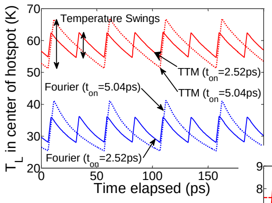


- Larger Source/Drain (S/D) volume will help heat spreading in drain
- BUT… no improvement for S/D thickness t_{SD} > 3-4 x t_{film} = Effect of parasitic side-wall capacitance on Intrinsic Delay
- Optimized, “well-behaved” GOI devices 30% faster than optimized SOI

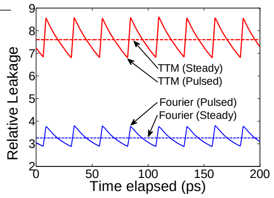
Transient Device Thermal Modeling

Z.-Y. Ong and E. Pop, *submitted* (2008)



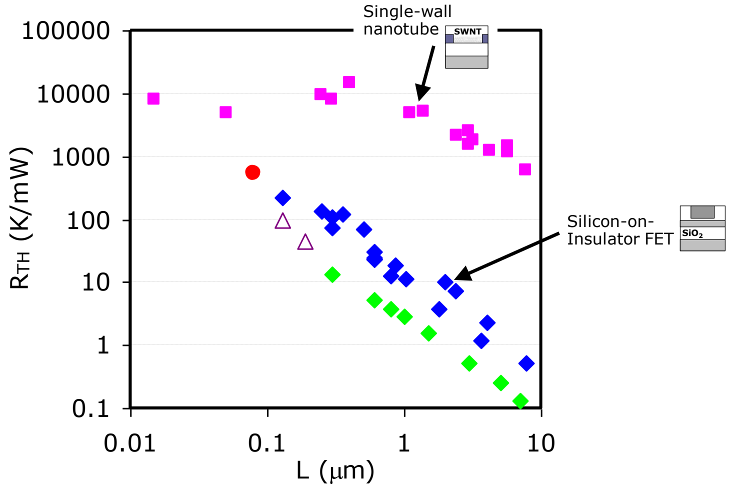


ITRS 2014 device specs



- Compact thermal device model including:
  - Non-equilibrium heat generation from Monte Carlo
  - Phonon relaxation parameter-matched to Boltzmann Transport Eq.
- Capture spatial and temporal temperature excursions
- What is the effect on leakage & reliability?

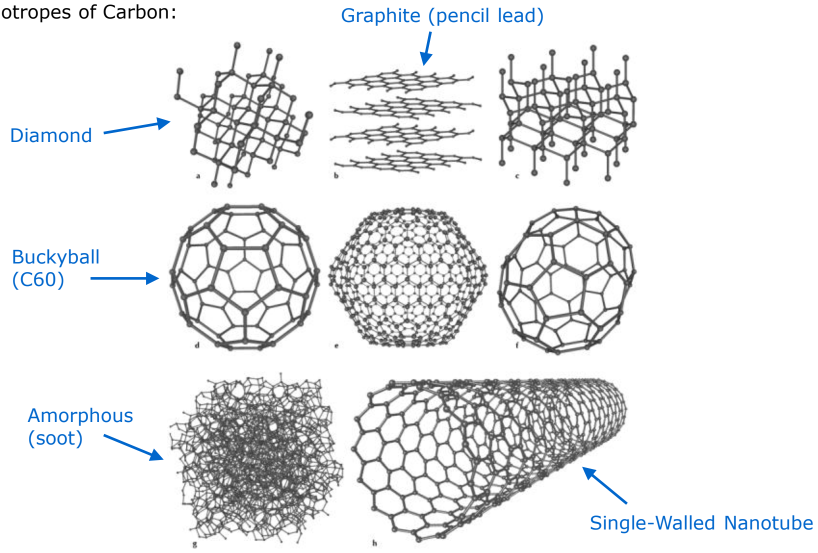
Onto Carbon Nanotubes…



Data: Mautry (1990), Bunyan (1992), Su (1994), Lee (1995), Jenkins (1995), Tenbroek (1996), Jin (2001), Reyboz (2004), Javey (2004), Seidel (2004), Pop (2004-6), Maune (2006).

Where Carbon Nanotubes Fit In

Allotropes of Carbon:



Graphite (pencil lead)

Diamond

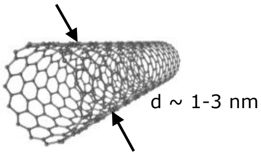
Buckyball
(C60)

Amorphous
(soot)

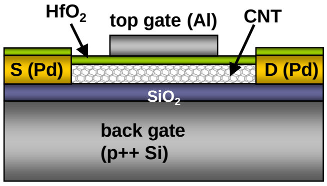
Single-Walled Nanotube

Carbon Nanotubes for Electronics

- Carbon nanotube = rolled up graphene sheet
- Great electrical properties
  - Semiconducting → Transistors
  - Metallic → Interconnects
  - Electrical Conductivity $\sigma \approx 100 \times \sigma_{Cu}$
  - Thermal Conductivity $k \approx k_{diamond} \approx 5 \times k_{Cu}$

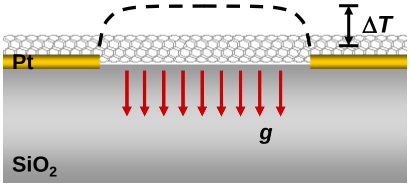


- Nanotube challenges:
  - Reproducible growth
  - Control of electrical and thermal properties
  - Going “from one to a billion”

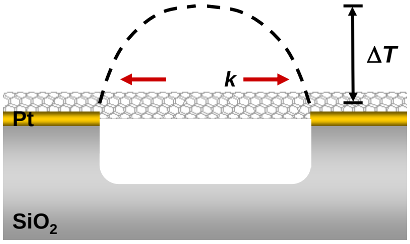


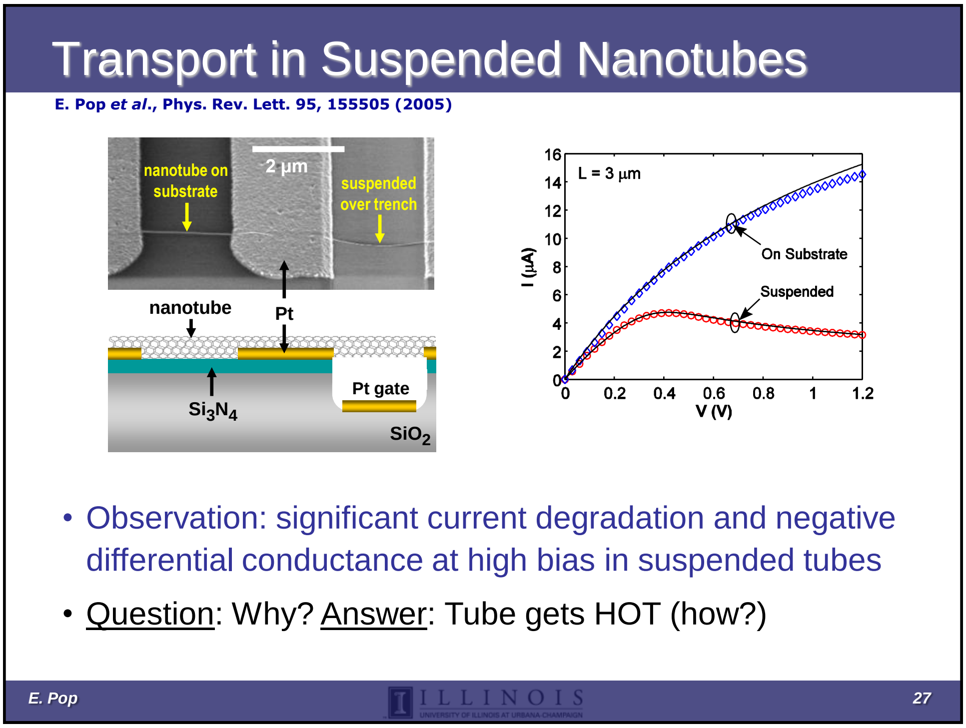
Nanotube Back-of-the-Envelope Estimates

- Typical $L \sim 2$ μm, $d \sim 2$ nm
- *On insulating solid substrate*
- Heat dissipated into substrate
  - Moderate power ~ 10 μW/μm
  - Peak $\Delta T \sim 60$ K



- Thermal conductivity $k \sim 3000$ W/m/K
- *Freely suspended nanotube*
- Heat dissipated along tube length
  - Moderate power ~ 10 μW (10 μA @ 1 V)
  - Peak $\Delta T \sim 400$ K!

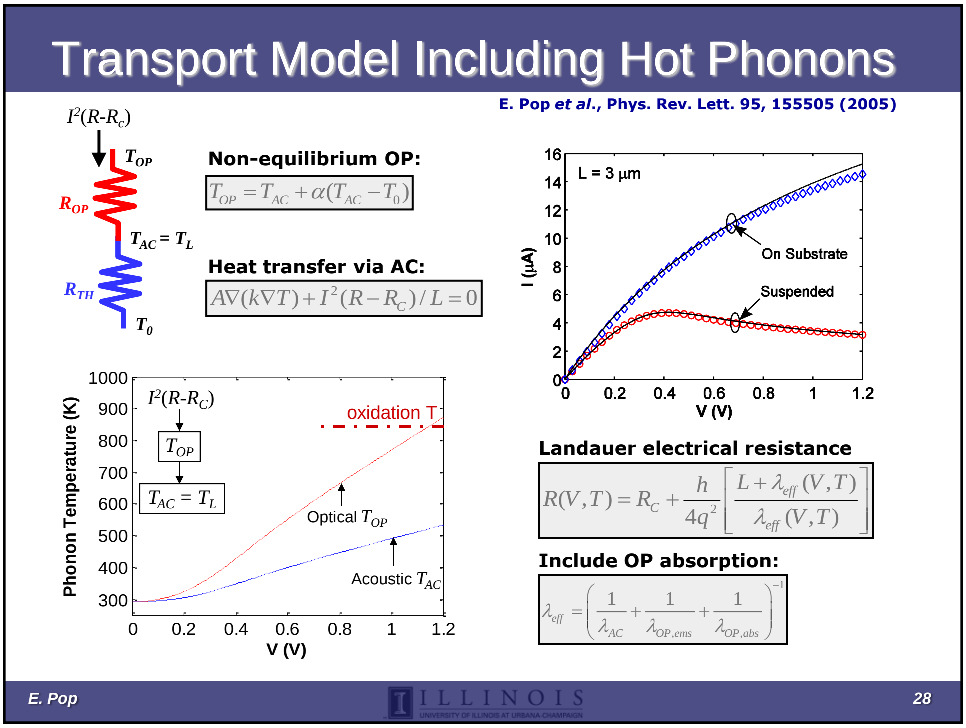




Transport in Suspended Nanotubes

E. Pop *et al.*, Phys. Rev. Lett. 95, 155505 (2005)

- Observation: significant current degradation and negative differential conductance at high bias in suspended tubes
- Question: Why? Answer: Tube gets HOT (how?)



Transport Model Including Hot Phonons

E. Pop *et al.*, Phys. Rev. Lett. 95, 155505 (2005)

Non-equilibrium OP:

$$T_{OP} = T_{AC} + \alpha(T_{AC} - T_0)$$

Heat transfer via AC:

$$A\nabla(k\nabla T) + I^2(R - R_C)/L = 0$$

Landauer electrical resistance

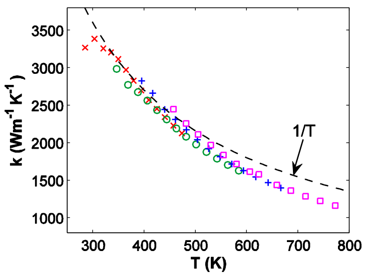
$$R(V,T) = R_C + \frac{h}{4q^2}\left[\frac{L + \lambda_{eff}(V,T)}{\lambda_{eff}(V,T)}\right]$$

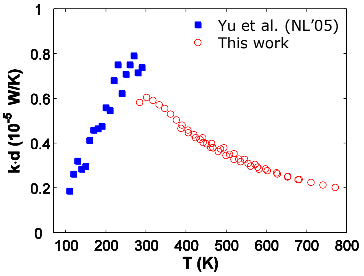
Include OP absorption:

$$\lambda_{eff} = \left(\frac{1}{\lambda_{AC}} + \frac{1}{\lambda_{OP,ems}} + \frac{1}{\lambda_{OP,abs}}\right)^{-1}$$

Extracting SWNT Thermal Conductivity

E. Pop *et al.*, *Nano Letters* 6, 96 (2006)



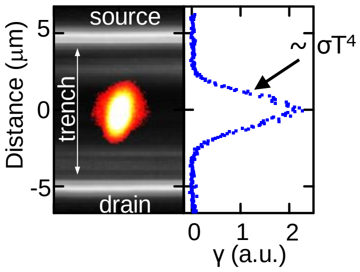


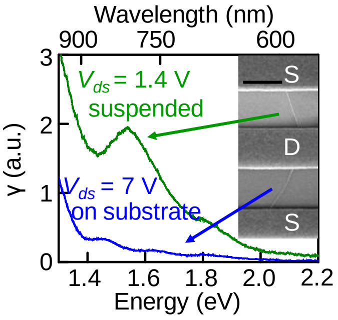
- "Inverse" numerical extraction of *k* from the high bias (*V* > 0.3 V) tail
- Comparison to data from 100-300 K of UT Austin group (C. Yu, *NL Sep'05*)
- Result: first "complete" picture of SWNT thermal conductivity from 100 – 800 K

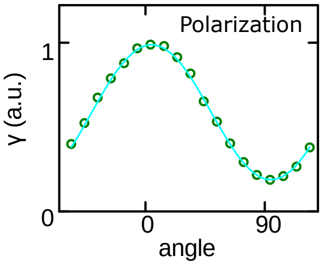
Light Emission from Metallic SWNTs

D. Mann *et al.*, *Nature Nano* 2, 33 (2007)

- Joule-heated tubes emit light:
  - Comes from center, highly polarized
  - Quasi-metallic = small band gaps
  - Emitted photons at higher energy than applied bias (high energy tail)



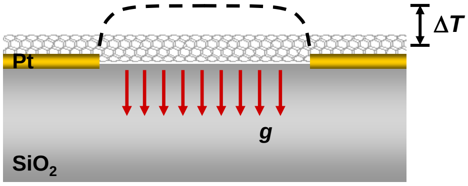




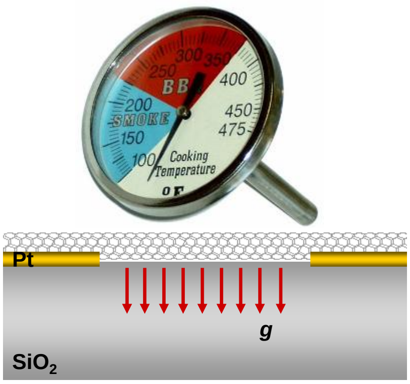
Return to SWNTs On Substrates

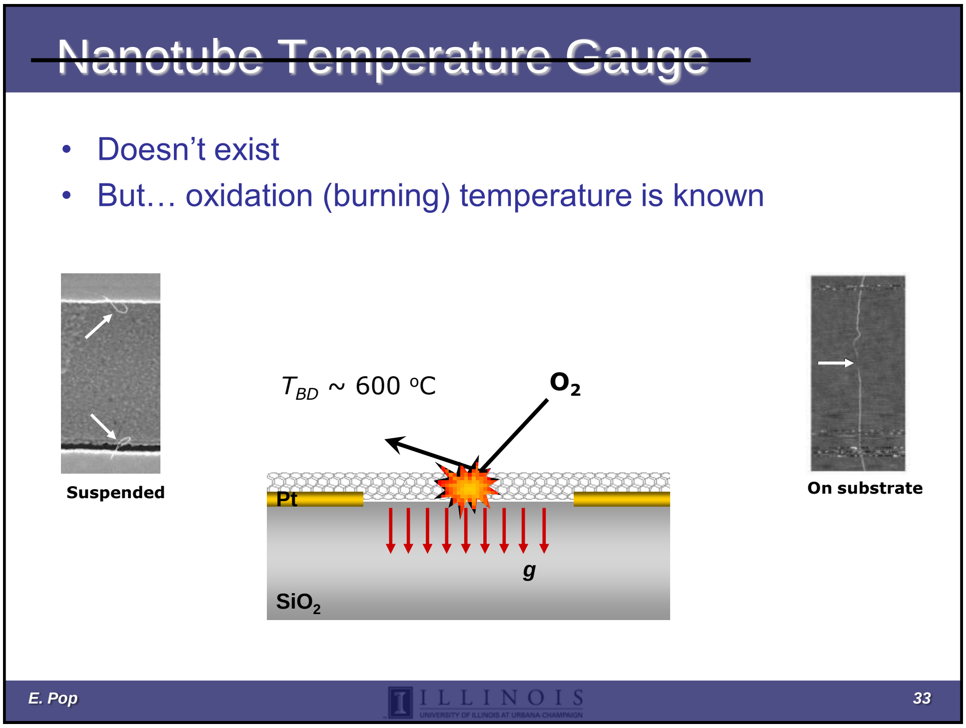
E. Pop *et al.*, Proc IEDM 2005; Proc IEEE 2006

- SWNT on insulating solid substrate
- Heat dissipated into substrate rather than along tube length
- *Q: How do I model heat loss into substrate?*
- [A: need some gauge of the tube temperature]



Nanotube Temperature Gauge





~~Nanotube Temperature Gauge~~

- Doesn't exist
- But… oxidation (burning) temperature is known

Suspended

T_{BD} ~ 600 °C

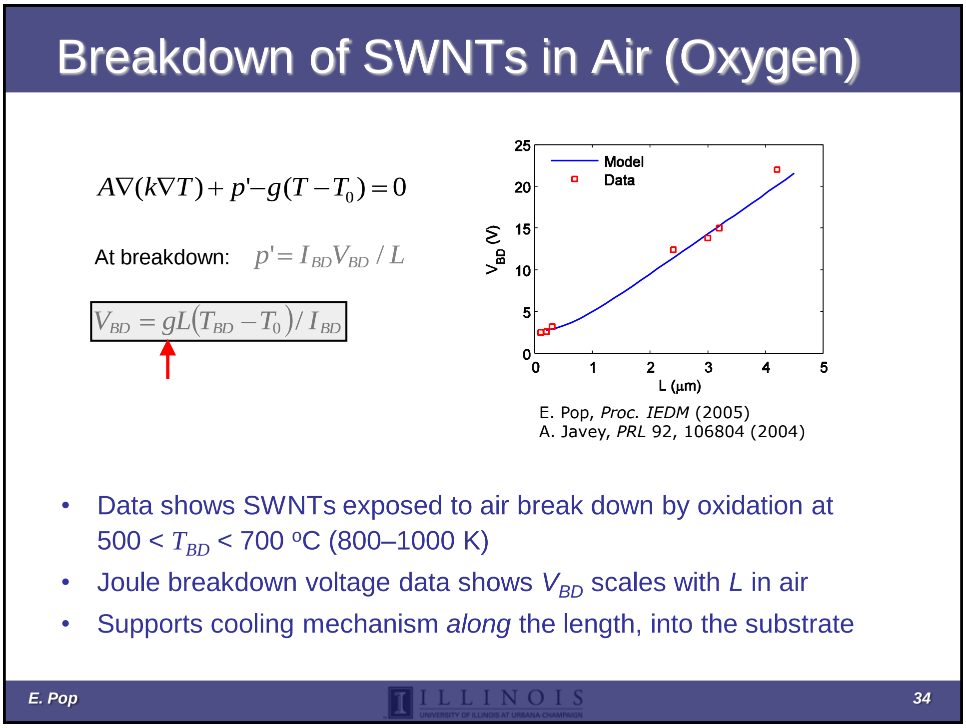
O_2

Pt

g

SiO_2

On substrate



Breakdown of SWNTs in Air (Oxygen)

$$A\nabla(k\nabla T) + p' - g(T - T_0) = 0$$

At breakdown: $p' = I_{BD}V_{BD}/L$

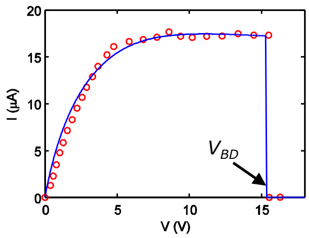
$$\boxed{V_{BD} = gL(T_{BD} - T_0)/I_{BD}}$$

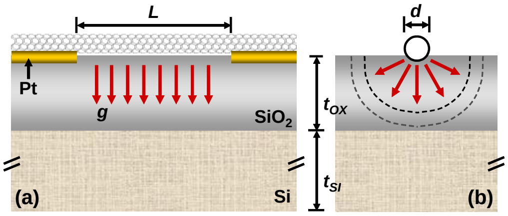
E. Pop, *Proc. IEDM* (2005)
A. Javey, *PRL* 92, 106804 (2004)

- Data shows SWNTs exposed to air break down by oxidation at 500 < T_{BD} < 700 °C (800–1000 K)
- Joule breakdown voltage data shows V_{BD} scales with L in air
- Supports cooling mechanism *along* the length, into the substrate

Electrical Breakdown of SWNTs

E. Pop *et al.*, J. Appl. Phys. 101, 093710 (2007)

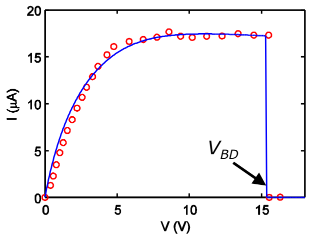


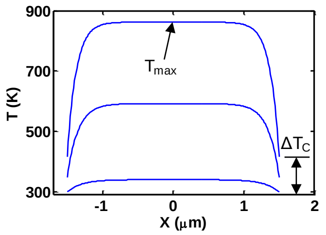


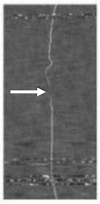
- SWNT exposed to air from the top
- Sweep voltage low to high
- Temperature peaks in the middle
- When $T_{max} = T_{BD} \rightarrow V = V_{BD}$ *and* $P_{BD} = I_{BD}V_{BD}$

Electrical Breakdown of SWNTs

E. Pop *et al.*, J. Appl. Phys. 101, 093710 (2007)







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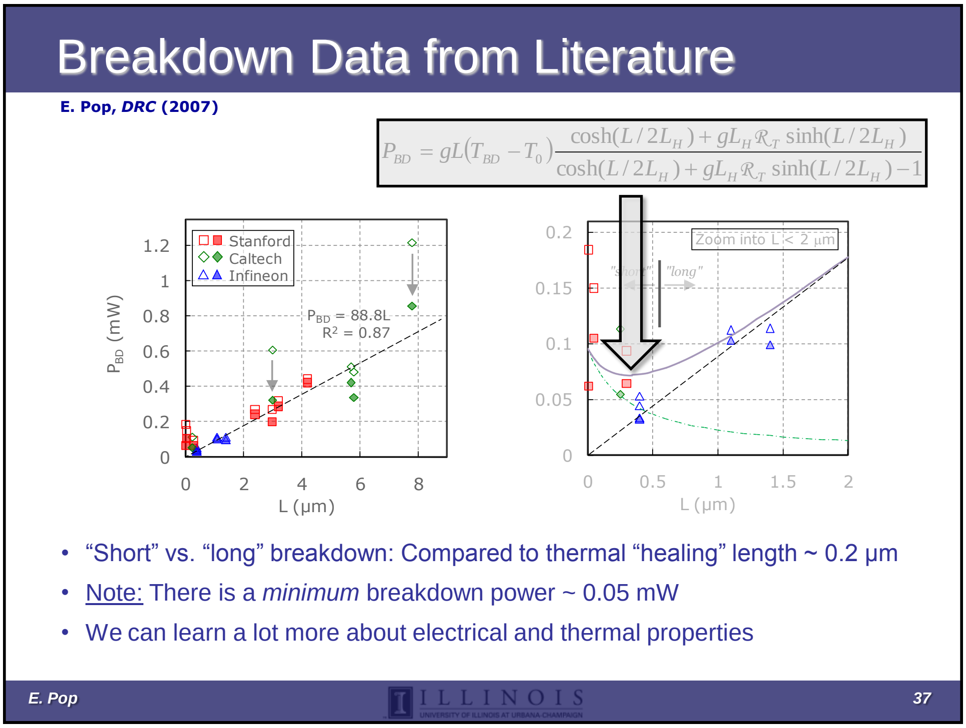


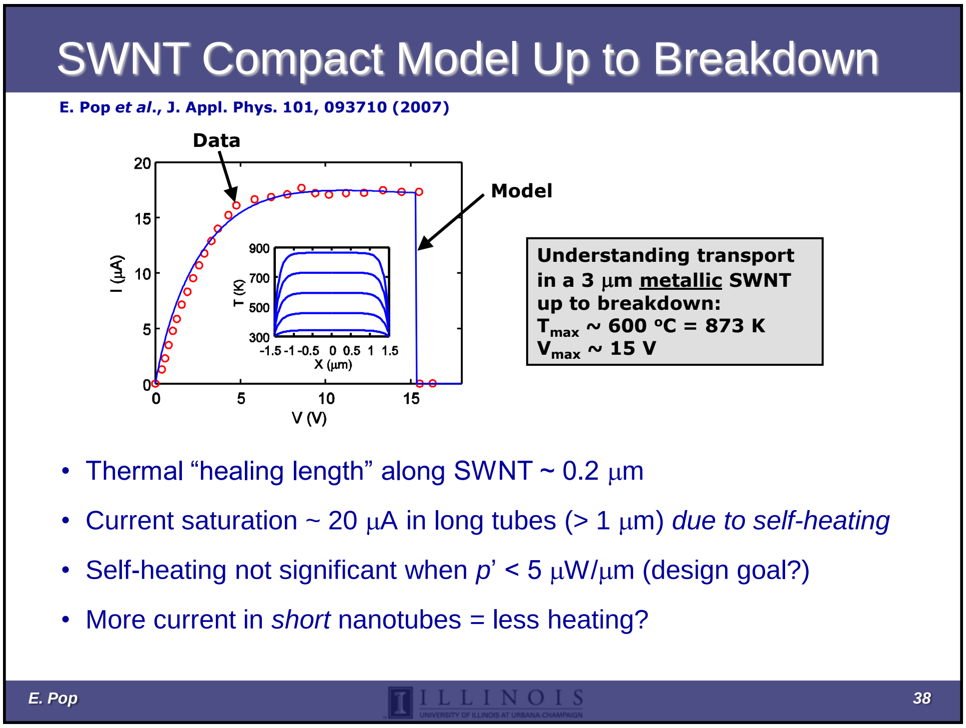
Breakdown Data from Literature

E. Pop, *DRC* (2007)

$$P_{BD} = gL(T_{BD} - T_0)\frac{\cosh(L/2L_H) + gL_H\mathcal{R}_T\sinh(L/2L_H)}{\cosh(L/2L_H) + gL_H\mathcal{R}_T\sinh(L/2L_H) - 1}$$

- “Short” vs. “long” breakdown: Compared to thermal “healing” length ~ 0.2 µm
- Note: There is a *minimum* breakdown power ~ 0.05 mW
- We can learn a lot more about electrical and thermal properties

E. Pop ILLINOIS UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN



SWNT Compact Model Up to Breakdown

E. Pop *et al.*, J. Appl. Phys. 101, 093710 (2007)

Understanding transport in a 3 µm metallic SWNT up to breakdown:
T_{max} ~ 600 °C = 873 K
V_{max} ~ 15 V

- Thermal “healing length” along SWNT ~ 0.2 µm
- Current saturation ~ 20 µA in long tubes (> 1 µm) *due to self-heating*
- Self-heating not significant when *p*’ < 5 µW/µm (design goal?)
- More current in *short* nanotubes = less heating?

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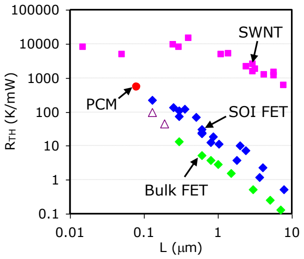
Summary



- Small device dimensions, high local power densities
- Increased device thermal resistance with decreasing dimensions
- Physics-based models to capture:
  - Size effects
  - Phonon non-equilibrium
  - Transient temperature effects
- Opportunity for "bottom-up" thermal device and materials design

http://poplab.ece.uiuc.edu