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Localized Heating and Switching in $MoTe_2$-Based Resistive Memory Devices

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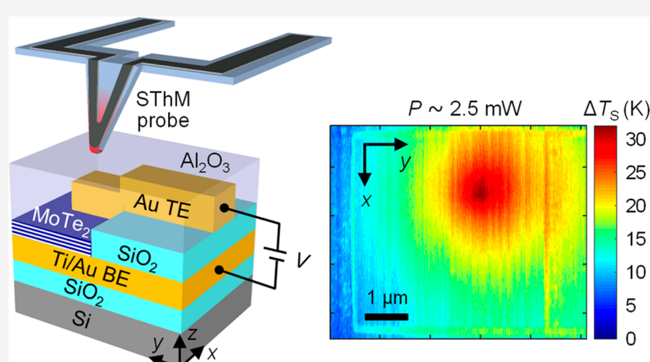
ABSTRACT: Two-dimensional (2D) materials have recently been incorporated into resistive memory devices because of their atomically thin nature, but their switching mechanism is not yet well understood. Here we study bipolar switching in $MoTe_2$-based resistive memory of varying thickness and electrode area. Using scanning thermal microscopy (SThM), we map the surface temperature of the devices under bias, revealing clear evidence of localized heating at conductive "plugs" formed during switching. The SThM measurements are correlated to electro-thermal simulations, yielding a range of plug diameters (250 to 350 nm) and temperatures at constant bias and during switching. Transmission electron microscopy images reveal these plugs result from atomic migration between electrodes, which is a thermally-activated process. However, the initial forming may be caused by defect generation or Te migration within the $MoTe_2$. This study provides the first thermal and localized switching insights into the operation of such resistive memory and demonstrates a thermal microscopy technique that can be applied to a wide variety of traditional and emerging memory devices.



KEYWORDS: *$MoTe_2$, 2D materials, resistive memory, bipolar switching, scanning thermal microscopy, localized heating*

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Two-dimensional (2D) materials have gained much interest in the past decade for scaled electronics and optoelectronics because of their tunable electrical, optical, and thermal properties.[1−3] More recently, they have been incorporated into memory devices,[4] either as heat confinement layers in phase change memory (PCM)[5,6] or as switching layers in resistive memory.[7−12] Transition metal dichalcogenides (TMDs), a class of 2D materials, have been suggested for phase engineering applications because many Group VI TMDs can exist in both semiconducting and metallic phases.[13,14] Molybdenum ditelluride ($MoTe_2$) is particularly interesting for these applications because it was predicted to have the lowest-energy phase boundary between the semiconducting and metallic phases.[14] While some studies have demonstrated switching in TMD-based memory, the switching mechanism remains unclear and could result from a localized phase change, ion migration causing (reversible) conductive regions, or interactions with the electrodes.[7,10−12] The switching mechanism can either be thermal in nature like in PCM or have a thermally-activated component like in resistive random access memory (RRAM), yet such aspects have not been investigated to date in TMD-based memory devices.

In this work, we use scanning thermal microscopy (SThM) to examine the thermal origins of switching behavior in $MoTe_2$-based resistive memory devices with varying $MoTe_2$ thickness and electrode area. We obtain spatial temperature maps of these devices under electrical bias and find evidence of localized heating due to conductive plugs which form during switching. Because the SThM measurements only probe the temperature at the surface of the devices, we correlate our measurements to electro-thermal simulations to obtain insight into the size and temperature of the conductive region *within* the $MoTe_2$. We also perform cross-sectional transmission electron microscopy (TEM) of memory devices after switching and find that the conductive plugs likely result from contact metal (here gold, Au) migration between the top and bottom electrodes. However, control experiments on $MoTe_2$ devices with graphite electrodes also show forming, suggesting this is initially triggered by Te or defect migration, rather than only by Au conductive bridge formation.

Figure 1a shows a side-view schematic of the initial devices, which consist of layered $MoTe_2$ between Au electrodes. The bottom and top electrodes (BE and TE) are patterned by electron beam (e-beam) lithography and deposited by e-beam evaporation with thicknesses of 45 nm (including a 5 nm titanium sticking layer under the Au) and 80 nm, respectively. The $MoTe_2$ is grown by chemical vapor transport (CVT),

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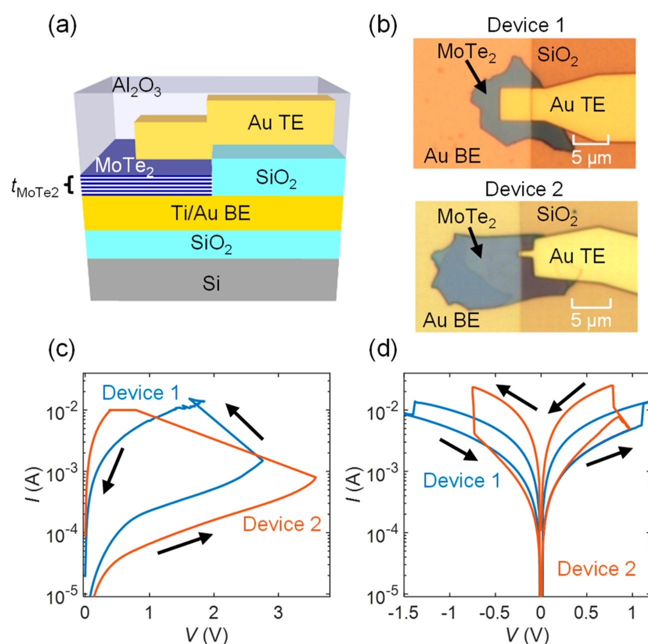

Figure 1. (a) Side-view schematic of $MoTe_2$ devices with a SiO_2 isolation layer between the Au top and bottom electrodes, as well as an Al_2O_3 capping layer. The BE has a 5 nm Ti sticking layer to improve adhesion of the Au to the SiO_2/Si substrate. (b) Top-down optical images of two devices, Device 1 ($t_{MoTe2} \sim 30$ nm) and Device 2 ($t_{MoTe2} \sim 55$ nm) with top electrode areas of 4.5×4.5 μm^2 and 0.7×0.4 μm^2, respectively. (c) Measured $I-V$ characteristics showing initial forming of Devices 1 and 2, with the arrows corresponding to the voltage sweep direction. (d) Measured $I-V$ characteristics showing subsequent bipolar switching of Devices 1 and 2.

which yields bulk crystals.[15,16] Thin layers (~10−55 nm thick) of $MoTe_2$ are mechanically exfoliated onto SiO_2/Si substrates and subsequently transferred onto Au BEs by a dry transfer process (see Supporting Information Section 1 for details). E-beam evaporated SiO_2 (~65 nm) is used to electrically isolate the two electrodes, and Al_2O_3 (~10 nm) deposited by atomic layer deposition (ALD) is used as a protective capping layer[17] above the TE, as shown in Figure 1a. The exfoliation, transfer, metal lift-off, and ALD steps are all performed in a N_2 glovebox with <3 ppm of O_2 and <1 ppm of H_2O to prevent surface oxidation of the $MoTe_2$.

Figure 1b displays optical images of two $MoTe_2$ devices (Device 1 and Device 2). Device 1 has Au TE area of 4.5×4.5 μm^2 and $MoTe_2$ thickness $t_{MoTe2} \sim 30$ nm, while Device 2 has Au TE area of 0.7×0.4 μm^2 and $t_{MoTe2} \sim 55$ nm. Figure 1c,d shows measured direct current vs voltage ($I-V$) curves of the two devices, with the arrows illustrating the direction of the voltage sweep. The devices typically have initial resistances of 1 kΩ to 1 MΩ (depending on TE area and t_{MoTe2}). We use a modified three-dimensional (3D) Poole−Frenkel model[18−20] to fit our $I-V$ curves during the forward sweep, as shown in Supporting Information Figure S1. At higher voltages, the devices undergo a "forming" step during a DC $I-V$ sweep. We use a current compliance (10 μA to 10 mA) and external series resistor (0.2 to 1 kΩ) to limit the amount of current. The devices transition to a low resistance state (LRS) with resistances R_{LRS} = 40 to 800 Ω, depending on the current compliance and series resistance used. When a voltage sweep of the opposite polarity is performed, the devices switch to a high resistance state (HRS) (the "RESET" step), and they transition back to the LRS after the polarity of the sweep is reversed again (the "SET" step). Figure 1d shows bipolar switching of Devices 1 and 2. We measured ~20 devices with similar forming and bipolar switching. We also present data on forming current, forming voltage, and R_{LRS} for devices with varying t_{MoTe2} and TE area in Supporting Information Figure S2.

To gain insight into the thermal origins of the device switching behavior, we use scanning thermal microscopy (SThM). SThM is an atomic force microscope (AFM) technique wherein a specialized AFM probe (here a temperature-dependent Pd resistor on a V-shaped SiN tip) is used in physical contact with a device to measure its surface temperature.[21−23] A voltage applied to the device induces Joule heating, which in turn causes the SThM probe to heat up. The electrical resistance of the probe changes with temperature, leading to a change in the output voltage (ΔV_{SThM}) of the SThM. ΔV_{SThM} is proportional to the temperature rise of the device surface (ΔT_S) above the ambient. The spatial resolution of these SThM probes is typically ~100 nm (depending on environmental conditions and calibration),[21−25] making it preferable to other techniques such as gate resistance thermometry, which gives average device temperature,[26] or Raman thermometry, which has good material selectivity but a diffraction-limited spatial resolution of ~0.5 μm.[22,25] (See Section 4 of the Supporting Information for measurement details, a discussion of spatial resolution, and calibration between ΔV_{SThM} and ΔT_S.)

Figure 2a shows a schematic of the setup, with the SThM probe on top of the Al_2O_3 surface. The Al_2O_3 (or some other

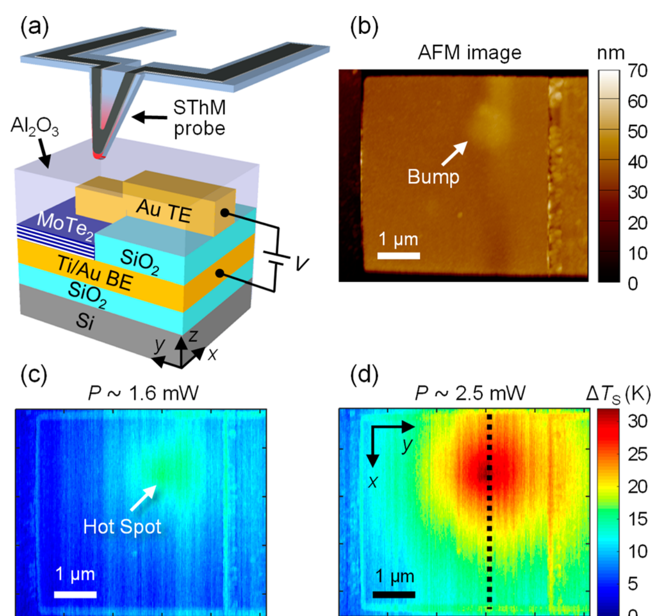

Figure 2. (a) Schematic of SThM setup, showing the probe on the surface of the Al_2O_3 capping layer and above the Au TE region. (b) AFM image of the top electrode region of Device 1, which is in the low resistance state. SThM images of Device 1 at power inputs of (c) $P \sim 1.6$ mW and (d) $P \sim 2.5$ mW. The color bar shows the temperature rise at the surface of the Al_2O_3 (ΔT_S), which was obtained using a calibration factor of 6.5 mV/K. The hot spots seen in (c) and (d) correspond to the bump on the top electrode in (b) and show evidence of localized heating due to a conductive plug in the device. The edges of the TE and SiO_2 can be seen because the SThM signal is affected by the topography of the sample.

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insulator) is needed to electrically isolate the probe and the TE. Figure 2b displays an AFM image of the TE region of Device 1 (in the LRS), illustrating a bump (~15 nm high) that emerged on the Au TE after the forming step. An SThM image is simultaneously taken with no bias applied to the device and is used to flatten all subsequent images at nonzero bias (see Supporting Information Figure S3 and Section 4 for details). We then apply a voltage to the TE while grounding the BE (without a series resistor), as illustrated in Figure 2a. Figure 2c,d shows SThM images of Device 1 with input power $P \sim 1.6$ mW and 2.5 mW, respectively, and the color bar shows the ΔT_S range (0−30 K) using a calibration factor $F = \Delta V_{SThM}/\Delta T_S = 6.5 \pm 0.5$ mV/K.[24] The images show a hot spot on the TE, matching the location of the bump in Figure 2b, becoming larger and hotter as we increase the input power. This localized heating suggests the formation of a conductive plug, and similar results have been observed for ~10 other devices. We point out that this is the first direct observation of localized switching visualized through thermal mapping TMD-based memory devices.

Next, we correlate our experimental results to 3D electro-thermal simulations performed using finite element modeling (COMSOL Multiphysics). These simulations allow us to estimate the temperature of the conductive plug during operation as well as the plug diameter (d_{plug}), based on the surface temperature obtained by SThM. Section 5 of the Supporting Information contains details of the simulations, and Table S1 shows the various parameters used. Figure 3a shows the ΔT_S profile of Device 1 along the black dashed line in Figure 2d. ΔT_S (red line) is again calculated using the calibration factor F, with the blue error bars showing the uncertainty in F. This temperature profile reveals broad heating of the entire TE, including $\Delta T_S > 15$ K at the edges, due to significant lateral heat spreading.

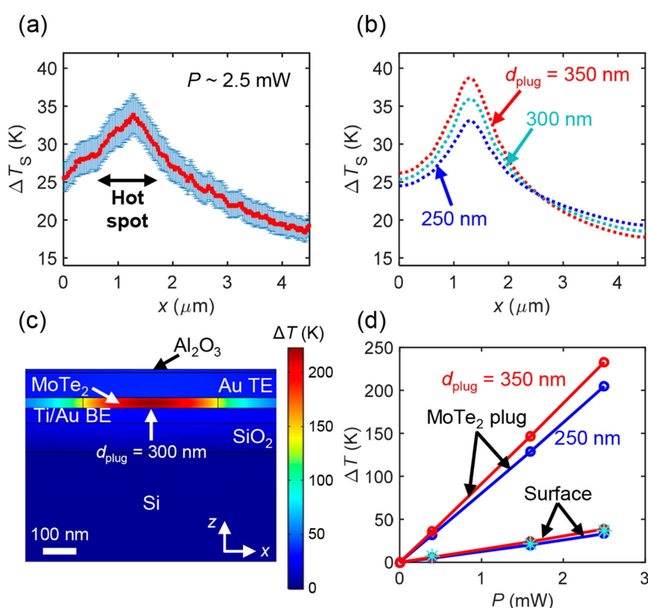

Figure 3. (a) Surface temperature profile from SThM measurement along the black dashed line in Figure 2d, with blue error bars. (b) Electro-thermal simulations of ΔT_S profiles for conductive plug diameters d_{plug} ranging from 250 to 350 nm at $P \sim 2.5$ mW. (c) Simulation of ΔT along cross-section of device at $P \sim 2.5$ mW for $d_{plug} = 300$ nm. (d) Simulated ΔT vs P for different d_{plug} inside the $MoTe_2$ plug and at the surface of the device. The cyan asterisks correspond to ΔT_S from SThM measurements.

We find that among the simulation parameters, the thermal boundary resistance (TBR) at the $MoTe_2$−Au interfaces plays a key role, yet it is among the least well-known inputs (e.g., compared to thermal conductivities of Au or SiO_2). The simulated ΔT_S profiles in Figure 3b show the closest agreement with the SThM data for TBR ≈ 70 m^2KGW^{-1} and d_{plug} from 250 to 350 nm. The estimated TBR is equivalent to a thermal boundary conductance (TBC = 1/TBR) of ~14 $MWm^{-2}K^{-1}$, which is very similar to that found for other 2D materials.[6,25] We note the peak ΔT_S increases with increasing d_{plug}, unlike in metal-oxide RRAM devices.[24] Our simulations suggest this behavior is due to the electrical conductivity of the plug being only ~100× higher than that of the surrounding $MoTe_2$. In metal-oxide RRAM, however, the conductive filament conductivity is $>10^{10}$ higher than that of the insulating metal-oxide surrounding it.[27,28] Therefore, the film surrounding the conductive plug in our devices also contributes to current conduction and heating.

Figure 3c shows a cross-sectional view of the simulated temperature distribution within the device for $d_{plug} = 300$ nm and $P = 2.5$ mW. The image has been cropped to focus on the conductive plug region (the silicon is actually 20 μm thick in our simulations, which is sufficient to fully capture the 3D heat spreading). As expected, the hottest region is in the $MoTe_2$ where the conductive plug is formed, with a peak $\Delta T_{plug} \approx 223$ K. There is substantial heat dissipation into the electrodes and the substrate, resulting in much cooler temperatures at the top and bottom surfaces. The simulated surface and $MoTe_2$ plug temperature rise ΔT, as well as ΔT_S from SThM measurements (cyan asterisks), for different power inputs are displayed in Figure 3d. At $P = 2.5$ mW, the peak ΔT_S ranges from ~33 to 39 K (corresponding to the SThM measurements), while the estimated peak ΔT_{plug} ranges from ~200 to 235 K for the different plug diameters. ΔT_{plug} has a larger range because it is more sensitive to plug diameter than ΔT_S. Heat dissipation in the TE also limits our ability to accurately extract ΔT_{plug}, which could be better estimated by reducing the TE thickness in future work. (The thicknesses of the $MoTe_2$ and top SiO_2 layers should also be reduced, due to required step coverage.)

In addition to steady-state measurements, we also sweep the voltage while holding the SThM probe stationary and in contact with the device surface directly above the conductive plug. This allows us to measure ΔT_S while switching the device between the LRS and HRS. Figure 4a shows an optical image of Device 3 with $t_{MoTe2} \sim 27$ nm and TE area of 2.5 × 2.6 μm^2. The $I-V$ measurements during bipolar switching (using an external series resistance of 220 Ω) and the corresponding ΔT_S from SThM are displayed in Figure 4b,c. The curves in Figure 4b are labeled with "SET" or "RESET," corresponding to a transition to the LRS or HRS, respectively. ΔT_S reaches between 50 and 115 K when the device switches between the two states. Assuming d_{plug} between 250 and 400 nm, we use our simulations to estimate the maximum T_{plug} during the first RESET and SET measurements to be ~650−750 K and ~530−630 K, respectively. During the second RESET and SET measurements T_{plug} is estimated to be ~700−850 K and 650−800 K, respectively. We note that SThM measurements cannot capture fast temperature transients (the thermal time constant of Pd-based probes is ~300 μs[23] and the sampling time of our SThM system is ~3 ms), so the plug and surface may reach even higher temperatures (and possibly the semiconducting-to-

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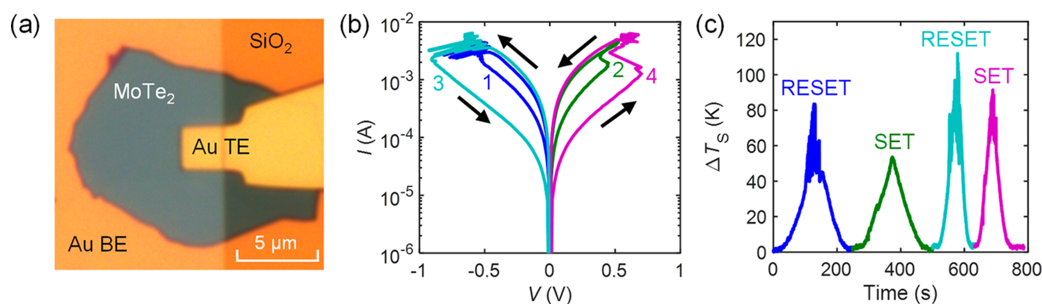

Figure 4. (a) Optical image of Device 3 with t_{MoTe2} ~ 27 nm and TE area of 2.5 × 2.6 μm^2. (b) $I-V$ measurements of Device 3 showing 2 switching cycles (with a series resistance of 220 Ω). The number next to each curve corresponds to the order of the measurements. (c) ΔT_S from SThM measurements as a function of time, taken simultaneously with the $I-V$ measurements in (b) of the same color. ΔT_S was calculated from ΔV_{SThM} using a calibration factor of 6.5 mV/K.

metallic transition temperature[29−31] for $MoTe_2$, ~ 920−1170 K) during bipolar switching.

To determine the effect of temperature on forming voltage, we also take temperature-dependent electrical measurements of a $MoTe_2$ device with Au electrodes (Device 4, t_{MoTe2} ~ 16 nm and TE area of 0.45 × 0.9 μm^2) using a fixed voltage range of 0 to 2 V and an external series resistance of 1 kΩ. At ambient temperatures of 300 and 400 K, the device remains in the unformed state following forward−backward $I-V$ sweeps. After increasing the temperature to 500 K, we observed device forming at ~1.3 V (see Supporting Information Figure S4). These measurements, in addition to the SThM measurements above, reveal that the forming mechanism has a thermally-activated component.

Next, we perform transmission electron microscopy (TEM) and energy dispersive spectroscopy (EDS) of Device 2 after switching. The device was cross-sectioned at the location of the conductive plug, which was determined by SThM, as shown in Supporting Information Figure S5. Figure 5a shows the TEM image of Device 2 across its active region, which was switched to the HRS before TEM imaging. Figure 5b−d shows EDS elemental intensity maps of Au, Mo, and Te, respectively. These maps reveal Mo and Te vacancies near the edge of the Au TE and Au within the $MoTe_2$ layer, suggesting that Au has migrated from one electrode to the other, displacing Mo and Te atoms. This migration likely results in the bump seen in the AFM image of Figure 2b.

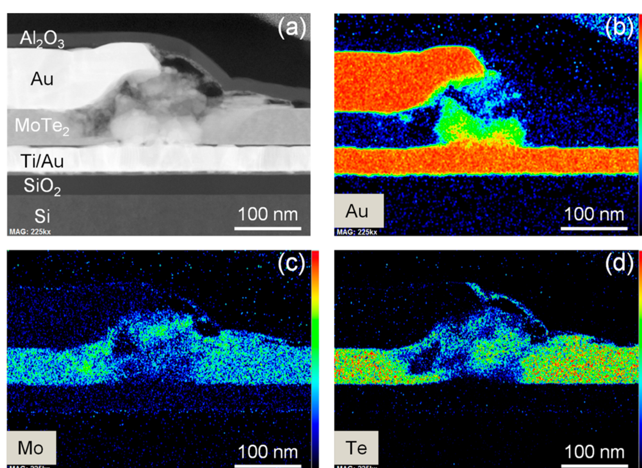

Figure 5. (a) High-angle annular dark-field (HAADF) transmission electron microscopy (TEM) cross-section of Device 2, which was switched to the high resistance state before imaging. The image shows the different layers of the device, including the $MoTe_2$ between the two Au electrodes, the underlying SiO_2/Si, and the Al_2O_3 capping layer. The layers above the Al_2O_3 are Pt and carbon coating layers to protect the samples during TEM preparation. Energy dispersive spectroscopy (EDS) elemental intensity maps showing (b) Au, (c) Mo, and (d) Te atoms. The color bars display the relative concentration of atoms, with red corresponding to the highest and black corresponding to the lowest.

We also see some evidence of O displacing Mo and Te atoms (Supporting Information Figure S6), which could be due to partial oxidation during fabrication. However, we do not expect O migration to be the primary cause of switching due to the low resistances measured in our devices, unlike in metal-oxide RRAM.[24] Switching in metal-oxide RRAM is often attributed to oxygen vacancies that form a conductive filament, which effectively reduces the device resistance.[32] We do not expect oxygen migration to reduce the resistance of our devices because MoO_x is more resistive than $MoTe_2$.[33]

SThM and TEM images of a different device (Device 5), initially in the LRS before TEM imaging, are shown in Figure S7 and S8, respectively. Mo and Te vacancies in the $MoTe_2$ film and Au diffusion between electrodes are similarly observed in these images. The Au migration, like metal ion migration in conductive bridge random access memory (CBRAM),[34,35] might explain the very low resistances measured (as low as ~40 Ω in some cases) when the devices are switched to the LRS (see Supporting Information Figure S2). During the RESET measurement, the Au bridge between electrodes likely breaks, causing an increase in resistance.

We note that Au migration has been observed in other thin film devices, including memory devices, from thermal stress during operation.[36,37] We estimate current densities over 10^5 A/cm^2 in the Au electrodes during the forming step and even higher during bipolar switching, which are sufficiently high to cause Au migration.[38,39] The Au migration can also occur at defects in the Au or in the $MoTe_2$,[12,40] where local current densities are larger. Though metal ion diffusion from the electrodes has often been reported in other types of devices and is of concern with regard to reliability in memory, this phenomenon has only recently been reported in TMD-based resistive memory devices.[11,12] We used Au electrodes in this study because it has often been used as a good contact metal to TMD semiconductors.[41,42] In addition, we found that $MoTe_2$ has good adhesion to Au during the transfer process due to the affinity of Au to chalcogen atoms.[43,44] (We observed that the $MoTe_2$ delaminates from other metals such as Pt or TiN during fabrication.)

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To test other conductive (but nonmetallic) electrodes, we also fabricate similar devices with graphite, which is an ultraflat semimetal, as the top and bottom electrodes. Supporting Information Figure S9a,b shows a schematic and optical image of such a device (Device 6) with t_{MoTe2} ∼ 29 nm, graphite bottom electrode thickness $t_{Gr,BE}$ ∼ 14 nm, graphite top electrode thickness $t_{Gr,TE}$ ∼ 5 nm, and TE area of ∼40 μm^2. $I-V$ measurements shown in Supporting Information Figure S9c reveal that at $V = 0.1$ V, the device has a resistance of ∼15 MΩ, and at ∼3.2 V it transitions to the LRS with ∼1.6 kΩ. A series resistor with $R = 1$ kΩ was used for these measurements. We were unable to RESET the device back to the HRS using either voltage polarity, possibly because of the additional series resistance of the graphite. The same behavior (stuck in LRS after forming) was reproduced on another device with graphite electrodes.

Thus, the different behavior between the devices with Au and graphite electrodes suggests, first, that initial forming of the $MoTe_2$ is not triggered by metal ion migration from the electrodes and, second, that further bipolar switching only in devices with Au electrodes is caused by conductive metal bridging, as seen in the TEMs discussed earlier. This mechanism is different from that of ref 10, which suggested bipolar switching due to localized phase change induced by an electric field. However, different initial forming and switching mechanisms among studies cannot be ruled out because there may be differences in sample quality (e.g., Te vacancies[45]) and processing (e.g., oxidation[46]). For example, a thin oxide layer on the $MoTe_2$ surface could rupture in a filamentary manner, leading to highly localized electric fields, current flow and subsequently a phase change in the pristine $MoTe_2$ beneath. Such an effect was recently observed in $Ge_2Sb_2Te_5$-based phase change memory with a thin oxidized electrode, which switched at lower current than control devices due to oxide filament formation.[6] (We do not expect such an oxide and such highly localized electric fields in our devices due to careful processing in a N_2 glovebox.) Other potential causes of forming could be defect (i.e., vacancy) generation or Te migration.[46,47] Immediately after forming, the current (and power) density is quite high, leading to significant Joule heating and causing Au migration, which is a thermally-activated process. Subsequent switching between the LRS and HRS is likely caused by the breaking and forming of these Au conductive plugs between the electrodes, as suggested by our cross-sectional TEMs.

In conclusion, we observed localized heating during operation of $MoTe_2$-based memory devices and measured their surface temperature using SThM for the first time. Together with temperature-dependent electrical data and TEM images, these SThM measurements reveal that both the forming and switching mechanisms have thermally-activated components. While the initial forming process may be caused by defect generation or Te migration, subsequent bipolar switching appears due to Au migration from the electrodes. Nevertheless, simulations suggest that high internal temperatures during switching could also cause localized phase change in the $MoTe_2$. Beyond this study, the SThM technique can also be applied to other traditional or emerging resistive memory devices to determine the location and temperature of switching regions, which is essential for understanding and optimizing such data storage.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.9b05272.

The 2D material transfer process; measurement and model of devices before forming; forming current and voltage data for all devices; scanning thermal microscopy (SThM) measurement details; 3D finite element modeling; temperature-dependent $I-V$ measurements; SThM images, TEM cross-sections, and EDS elemental maps; $MoTe_2$ device with graphite electrodes (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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Supporting Information

Localized Heating and Switching in $MoTe_2$-Based Resistive Memory Devices

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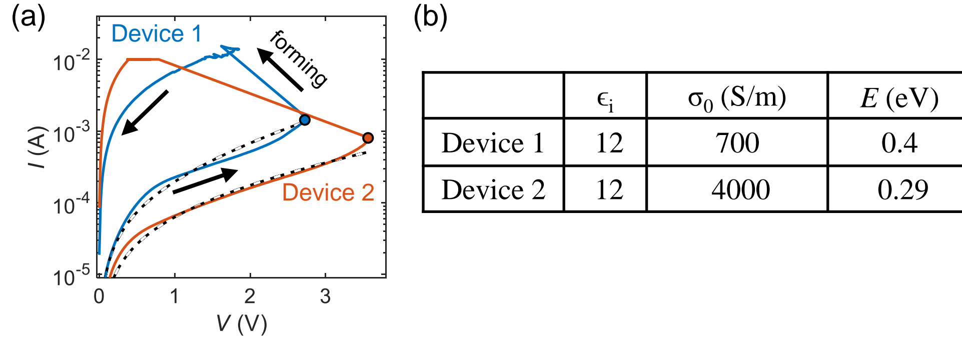
1. 2D Material Transfer Process

The procedure for transferring $MoTe_2$ (and graphite) layers that have been mechanically exfoliated onto SiO_2/Si chips is outlined below. A microscope with a heated stage and a micromanipulator inside a N_2 glovebox (with <3 ppm O_2 and <1 ppm H_2O) are needed to perform the transfer.

1. Spin-coat a thin layer of polypropylene carbonate (PPC) onto a hemispherical polydimethylsiloxane (PDMS) stamp, as in Ref. [1]. Attach PPC/PDMS stamp to a glass slide.
2. Place the 2D material sample on the stage inside the glovebox with carbon tape or other adhesive and find the flake of interest under the microscope.
3. Using the micromanipulator, lower the PPC/PDMS onto the 2D material sample until they are in contact.
4. Heat stage to 80°C and then allow it to cool down to 40°C.
5. Slowly lift the PPC/PDMS stamp from 2D material. The flake of interest should lift off of the SiO_2/Si chip and remain attached to the PPC/PDMS stamp.
6. Place target substrate on stage using carbon tape and find the region of interest.
7. Press PPC/PDMS stamp onto target sample until they are in contact.
8. Heat stage to 110°C and wait 5 minutes.
9. Slowly peel stamp off of the sample. The 2D material should remain on the target substrate.
10. Soak sample in acetone to remove PPC residue, rinse with IPA, and dry with a N_2 gun.

2. Measurement and Model of Devices before Forming

Figure S1 shows measured current vs. voltage (*I*-*V*) curves of Devices 1 and 2 from Figure 1 in the main text. A three-dimensional (3D) modified Poole-Frenkel equation,[2-3] which takes into account the effects of donors and traps, is used to model the conduction mechanism in these devices before forming. The fitting parameters used in the model are the high frequency relative dielectric constant ϵ_i of $MoTe_2$,[4] conductivity σ_0 (includes mobility, density of states, and donor and trap densities, as described in Ref. [2]), and activation energy *E*. The table in Figure S1b shows the fitting parameters used for Devices 1 and 2.



	ϵ_i	σ_0 (S/m)	*E* (eV)
Device 1	12	700	0.4
Device 2	12	4000	0.29

Figure S1. Measured *I*-*V* curves of Devices 1 and 2 from Figure 1 (solid colored lines), with data before forming fit to a modified 3D Poole-Frenkel equation (dashed black lines). Black arrows represent the measurement direction. The circled data points signify ($V_{forming}$, $I_{forming}$). (b) Fitting parameters from 3D Poole-Frenkel equation used to fit the *I*-*V* curves in (a).

3. Forming Current and Voltage Data for All Devices

Figure S2 shows forming current ($I_{forming}$) and forming voltage ($V_{forming}$) vs t_{MoTe2}, and low resistance state (R_{LRS}) vs. TE area for several $MoTe_2$ devices. $I_{forming}$ does not have a clear trend with increasing $MoTe_2$ thickness (t_{MoTe2}), while $V_{forming}$ increases with increasing t_{MoTe2}. The dashed line in Figure S2b is a linear fit to the data, with slope 0.04 V/nm, which is the average forming field, and y-intercept of 1.38 V. R_{LRS} has no dependence on top electrode (TE) area, which is further evidence that switching results in the formation of conductive plugs in these devices.

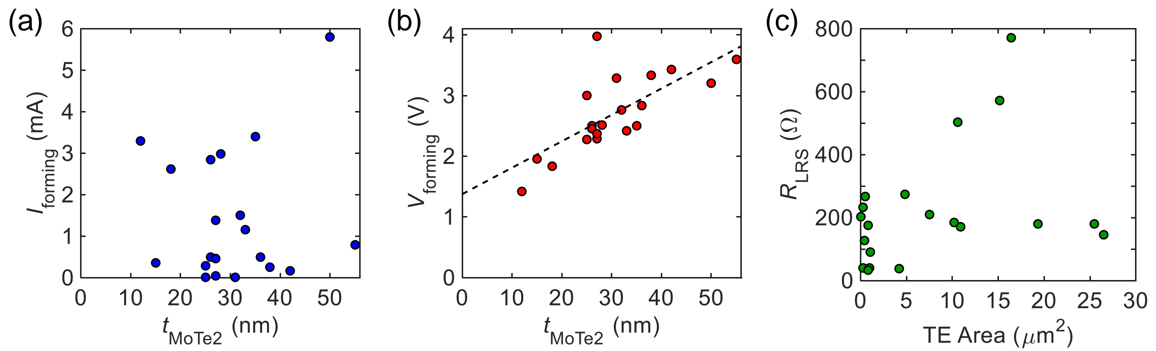


Figure S2. (a) Forming current ($I_{forming}$) vs. $MoTe_2$ thickness (t_{MoTe2}) for several $MoTe_2$ devices. (b) Forming voltage ($V_{forming}$) vs. t_{MoTe2}. The dashed line represents a linear fit. (c) Low resistance state R_{LRS} as a function of TE area for the same set of devices.

4. Scanning Thermal Microscopy (SThM) Measurement Details

a. Measurement details

We perform SThM measurements in passive mode with a bias of 0.5 V. The probes are model PR-EX-GLA-5 from Anasys Instruments, which are Pd-based with a resonant frequency of ~50 kHz and a spring constant of ~0.1 N/m. The scans are performed at a rate of 0.8 Hz and contact mode set point of 0.5 V, i.e. an estimated force of ~5 nN. We perform all measurements at room temperature in air with 20-30% humidity.

Measurements are either performed in steady-state, in which a constant voltage is applied to the device and the probe is scanned to obtain spatial temperature maps, or during device operation, in which the voltage is swept while the SThM probe is held in a ~10 nm × 10 nm area on the device surface above the hot spot.

b. Probe calibration process

We calibrate the SThM probe by measuring metal lines of varying nominal width (50 nm to 750 nm) with the same probe, and we convert the SThM voltage to temperature using the known temperature coefficient of resistance (TCR) of the metal lines. The metal lines are capped with an Al_2O_3 layer (comparable to the one on our memory devices) to account for similar capacitance effects and similar thermal (boundary) resistance at the probe-sample interface. The electrical capacitance coupling of the SThM to the device is also more than two orders of magnitude smaller than that of the memory device due to the large difference between the SThM probe area and the device area.

The calibration estimates the combined heat transport through direct heat conduction, convection, and a water meniscus at the probe-sample interface, resulting in an effective thermal exchange radius r_{th}. Our calibration yields a width-dependent calibration factor $F(w)$, which is constant for $w > 200$ nm but decreases for $w < 200$ nm (see Ref. [5], which uses the same calibrated probe as we use in our measurements). This suggests $r_{th} \sim 100$ nm, which is in good agreement with previous work by Puyoo *et al.*[6] Since our $MoTe_2$ device features are larger than 200 nm in this work, we use $F = 6.5 \pm 0.5$ mV/K.

We note that the calibration process must be performed for each probe used, and we can only obtain surface temperature estimates from SThM images taken with a calibrated probe. A probe can be used on many devices, depending on the surface roughness and measurement conditions. Our devices have low surface roughness (<2 nm) and we use the same measurement conditions across samples, so we find that we can take >100 thermal maps before the probe physically degrades and the SThM signal changes become evident.

c. Image flattening process

The SThM images typically have an offset and slope, even with no applied voltage. Using the SThM image at 0 V applied to the device (Figure S3a), we fit a line through one row of the data and subtract the slope from the image to flatten it. We repeat this process for one column of the data. Next, we subtract the offset from the image to bring the average V_{SThM} to 0 V. For all subsequent images at higher bias, we similarly flatten the images and subtract the offset using the values from the 0 V image. The SThM images shown in Figure 2c,d were flattened using this process.

We note that the edges of the TE appear clearly in the 0.65 V image (Figure S3b) and seem to heat up. However, since this nonzero SThM voltage is also measured at the edges of the electrodes during the 0 V scan (Figure S3a), we are confident that this is not a result of heating at the edges of the electrodes. Instead, this nonzero SThM voltage is observed at the edges because the measurement is affected by the topography of the sample.

We also point out that the gradual topography change from the bump on the TE in Figure 2b does not affect the SThM signal (and therefore the accuracy of the mapped temperature), as shown in Figure S3a. Only drastic topography changes, like the edges of our top electrode (~80 nm tall), appear to affect the SThM signal because the thermal exchange radius will be partially truncated while the SThM probe goes over a sharp step (see Figure 4 in Ref. [6]).

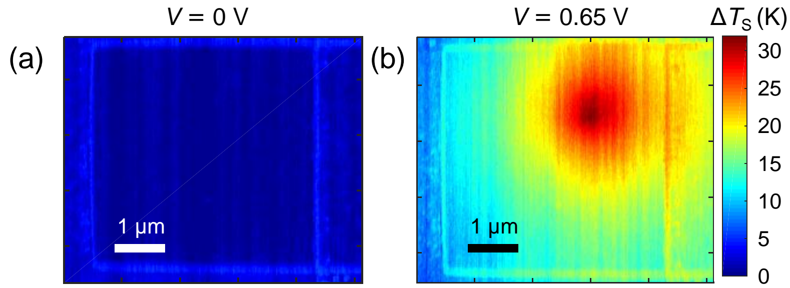


Figure S3. SThM image of Device 1 with applied voltage of (a) 0 V and (b) 0.65 V. The 0 V image is used to flatten all other SThM images taken on Device 1. The mapped temperature in the color bar is at the top of the Al_2O_3 layer (~10 nm) which covers this device.

5. 3D Finite Element Modeling

We recall that SThM measures the *surface* temperature at the top of the Al_2O_3 layer covering the devices. Thus, we perform 3D finite element electro-thermal simulations using COMSOL Multiphysics to estimate temperature rise *within* the plug (ΔT_{plug}) when the device is under bias, in addition to the diameter of the conductive plug (d_{plug}). An electrical model is used to apply a voltage between the TE and BE, and a thermal model is used to predict the temperature distribution. The two models are coupled via Joule heating and temperature-dependent material properties (see Table S1).

The bottom of the Si substrate is held at ambient temperature (T_0 = 293 K), and the outer boundaries are treated as insulated (adiabatic). We model the $MoTe_2$ layer as two regions, the conductive plug and the rest of the film, with different electrical conductivity values, σ_{plug} and σ_{film}. We assume a ratio $r_\sigma = \sigma_{plug}/\sigma_{film} = 100$ between the two regions, based on the change in resistance of our devices before and after forming. We model the plug and film resistances in parallel to obtain the measured $R_{LRS} \sim 167\ \Omega$ at $V = 0.65$ V for this device, as shown in Eq. (1):

$$R_{LRS} = \frac{t_{MoTe2}}{\sigma_{plug} A_{plug} + \sigma_{film} A_{film}} \quad (1)$$

We also include a temperature dependence in the $MoTe_2$ film electrical conductivity σ_{film}, based on exponential fits to electrical conductivity σ vs. T of unformed devices. The σ used for the $MoTe_2$ film and conductive plug in our simulation are given in Eqs. (2) and (3), respectively:

$$\sigma_{\text{film}} = \frac{t_{\text{MoTe2}}}{R_{\text{LRS}}(r_\sigma A_{\text{plug}} + A_{\text{film}})} e^{0.007(T-T_0)} \tag{2}$$

$$\sigma_{\text{plug}} = \frac{r_\sigma t_{\text{MoTe2}}}{R_{\text{LRS}}(r_\sigma A_{\text{plug}} + A_{\text{film}})} \tag{3}$$

The electrical conductivity of Au is $\sigma_{\text{Au}} = 1.4 \times 10^7$ S/m with a temperature dependence based on a measured temperature coefficient of resistance $\alpha = 0.0025$ K^{-1} for thin Au films.[7] The thermal conductivity of Au is estimated using the Wiedemann-Franz Law with $k_{\text{Au}} = \sigma_{\text{Au}} L_0 T$, where the Lorenz number is $L_0 = 2.44 \times 10^{-8}$ WΩK^{-2} (see Table S1 below).

The thermal boundary resistance (TBR) is applied at various interfaces to model heat fluxes and temperature gradients. The TBRs for Au-SiO_2 and SiO_2-Si interfaces are 10 m^{2}KGW^{-1} and 3 m^{2}KGW^{-1}, respectively.[8-9] We use the TBR of the $MoTe_2$-Au interfaces and d_{plug} as fitting parameters and find that a TBR of ~70 m^{2}KGW^{-1} and d_{plug} ranging from 250 to 350 nm yield the best fits to our experimental data within the error bars (see Figure 3a,b). We average ΔT_S from simulations across the thermal exchange radius of the SThM probe to get the expected Gaussian averaging from thermal measurements. From these simulations, we estimate the range of ΔT_{plug} for the different d_{plug} and applied voltage values.

Table S1. Material properties used in simulation, where T_0 = 293 K.

	σ (S/m)	**k (W/m/K)**
Au (electrode)	$1.4 \times 10^7/[1 + \alpha(T - T_0)]$	$\sigma_{\text{Au}} L_0 T$ (= 100 at 293 K)
SiO_2	1×10^{-12}	1.4 (Ref. [9])
Si	2×10^4 (for doping of 2×10^{19} cm^{-2})	95 (Refs. [10,11])
$MoTe_2$ (film)	See Equation (2)	10 (in plane) 1.5 (out of plane, Ref. [12])
$MoTe_2$ (plug)	See Equation (3)	

6. Temperature-Dependent *I-V* Measurements

We measure temperature-dependent *I-V* curves of a $MoTe_2$ device before forming, with t_{MoTe2} = 16 nm and TE area of 0.45 × 0.9 μm^2 (Device 4, shown in Figure S4a). We perform forward-backward sweep measurements at T_0 = 300 K, 400 K, and 500 K ambient temperature using a sweep range of 0 to 2 V and an external series resistance of 1 kΩ, as shown in Figure S4b. We fit the *I-V* curves (before forming) to a 3D modified Poole-Frenkel model, as in Figure S1, with ϵ_i = 10, σ_0 = 500 S/m, and E = 0.37 eV. At T_0 = 500 K ambient temperature, the device switches to the LRS at V = 1.3 V. These measurements underscore that the forming in our devices has a thermally-activated component.

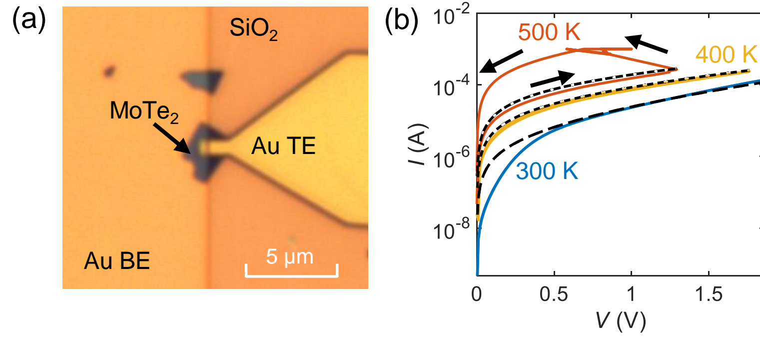


Figure S4. (a) Optical image of Device 4 with t_{MoTe2} = 16 nm and TE area of 0.45 × 0.9 μm^2. (b) Forward-backward *I-V* measurements from 0 to 2 V (with a series resistance of 1 kΩ) at varying ambient temperature (solid colored lines). The *I-V* data before forming are fit to a modified 3D Poole-Frenkel model (dashed black lines).

7. SThM Images, TEM Cross-sections, and EDS Elemental Maps

Figure S5 shows atomic force microscopy (AFM) and scanning thermal microscopy (SThM) images of Device 2 (with t_{MoTe2} = 55 nm and TE area of 0.7 × 0.4 μm^2), which was switched to the high resistance state. We use these SThM images to determine the location of the conductive plugs for the transmission electron microscopy (TEM) study. Therefore, we do not use a calibrated probe for these measurements since we only need qualitative thermal maps rather than surface temperature estimates. The TEM image and energy dispersive spectroscopy (EDS) elemental maps (extended version of Figure 5) are shown in Figure S6 for Device 2. We perform AFM and SThM as well as TEM and EDS on another device (Device 5), which was in the low resistance state, shown in Figures S7 and S8, respectively. Device 5 has t_{MoTe2} = 50 nm and TE area of 2.2 × 1.9 μm^2.

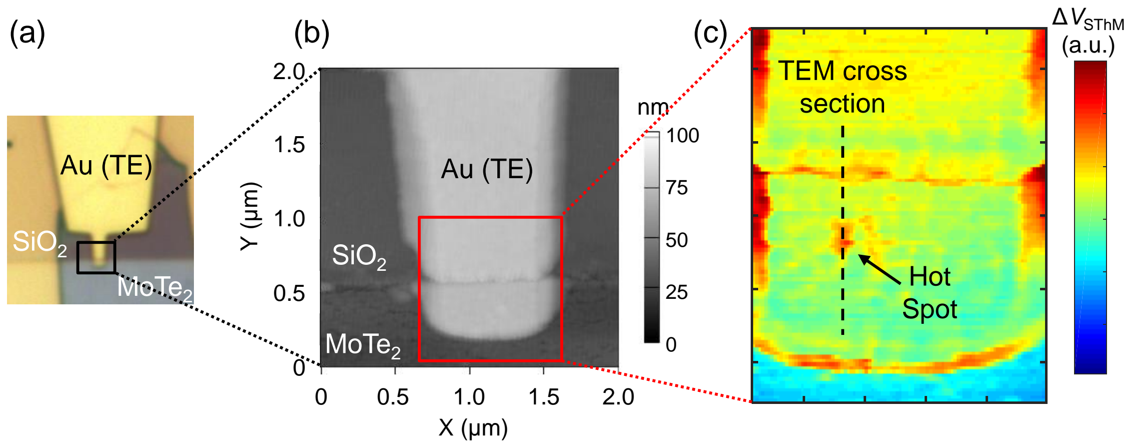


Figure S5. (a) Optical and (b) AFM images of Device 2. (c) SThM image showing the region of the device corresponding to the red box in (b). The vertical black dashed line is drawn along the hot spot (marked by arrow) where the TEM cross-section was taken, for Figure S6.

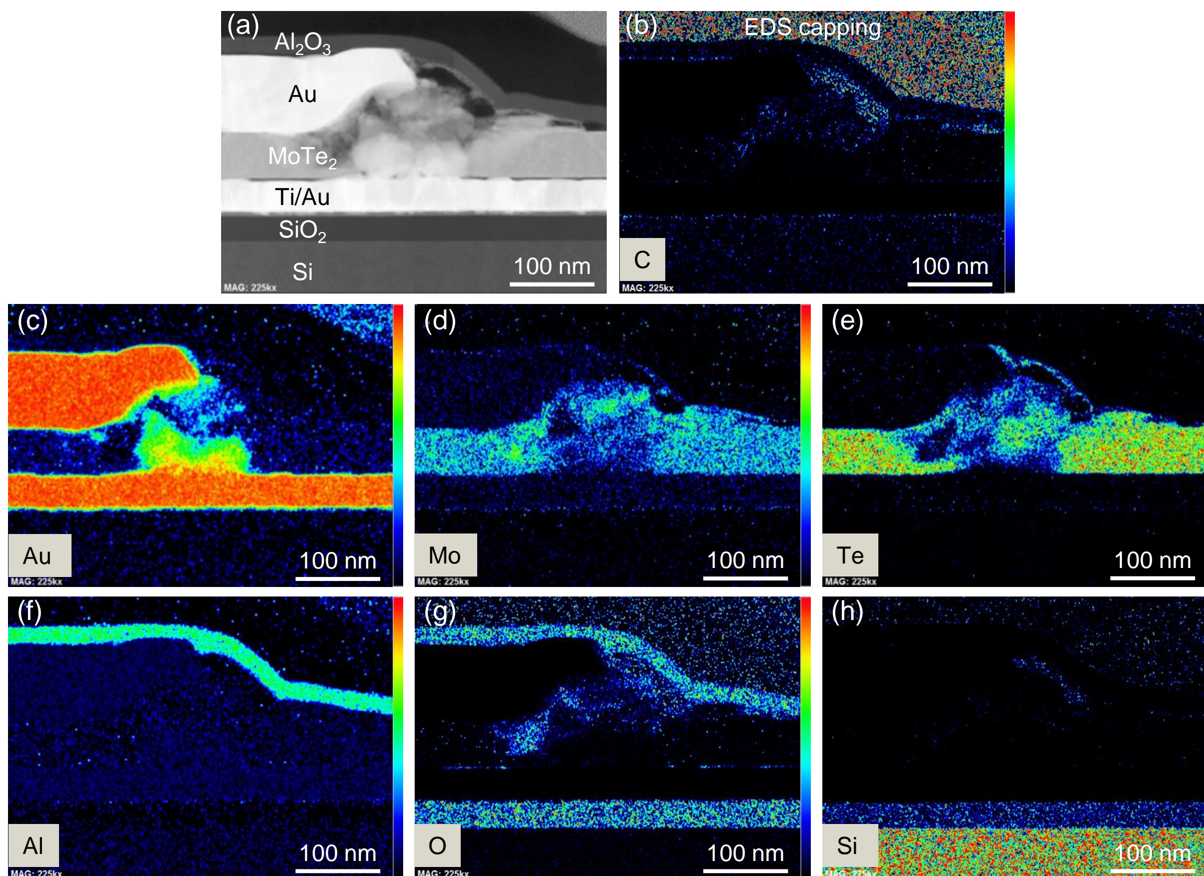


Figure S6. Extended version of Figure 5 from main text with additional elemental maps. (a) High-angle annular dark-field (HAADF) TEM cross-section of Device 2, which was switched to the high resistance state before imaging. EDS elemental intensity maps showing (b) C, (c) Au, (d) Mo, (e) Te, (f) Al, (g) O, and (h) Si. The color bar shows the relative concentration of atoms, with red corresponding to the highest and black corresponding to the lowest.

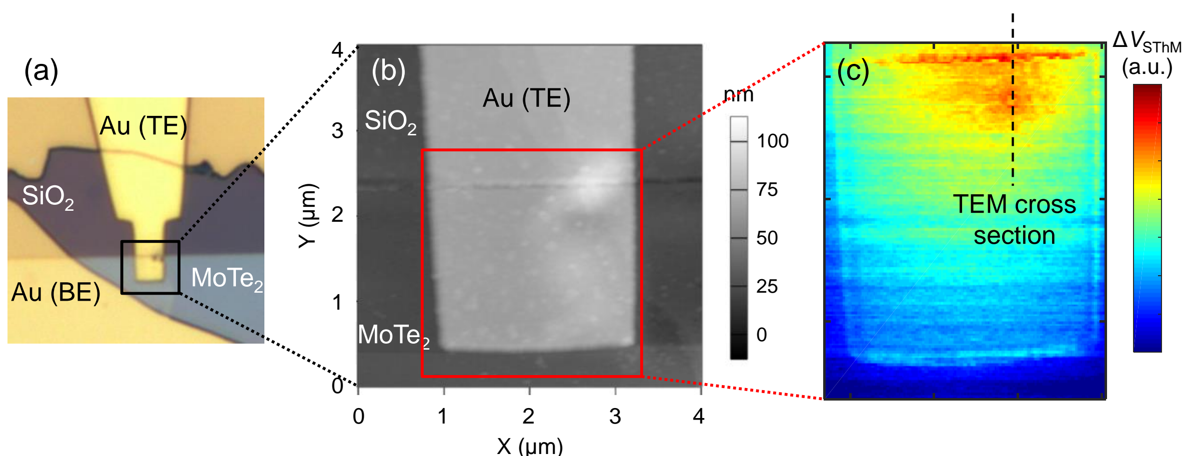


Figure S7. (a) Optical and (b) AFM images of Device 5 with t_{MoTe2} = 50 nm and TE area of 2.2 × 1.9 µm^2. (c) SThM image showing the region of the device corresponding to the red box in (b). The vertical black dashed line is drawn along the hot spot where the TEM cross-section was taken, for Figure S8.

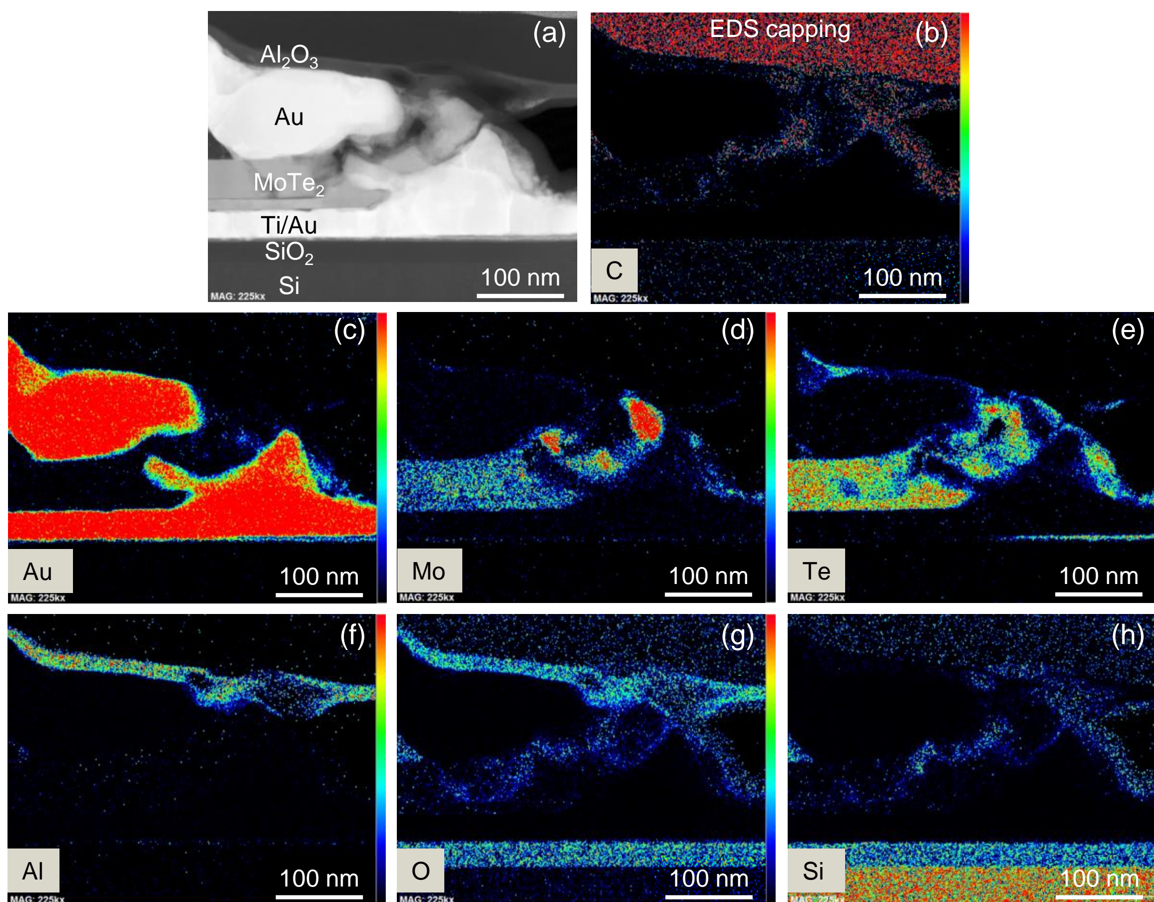


Figure S8. (a) HAADF TEM cross-section of Device 5, which was switched to the low resistance state before imaging. EDS elemental intensity maps showing (b) C, (c) Au, (d) Mo, (e) Te, (f) Al, (g) O, and (h) Si. The color bar shows the relative concentration of atoms, with red corresponding to the highest and black corresponding to the lowest.

8. $MoTe_2$ Device with Graphite Electrodes

Figure S9 shows the schematic, optical image, and *I-V* measurements of a $MoTe_2$ device with graphite electrodes (Device 6). The thicknesses of the $MoTe_2$, bottom graphite, and top graphite layers are ~29 nm, ~14 nm, and ~5 nm, respectively, and the graphite TE area is ~40 μm^2. The same transfer process used to transfer $MoTe_2$ films (described in Section 1) is used to transfer graphite films. At ~3.2 V, the device transitions to the low resistance state, demonstrating that forming in our $MoTe_2$ devices does not result from electrode metal ion migration.

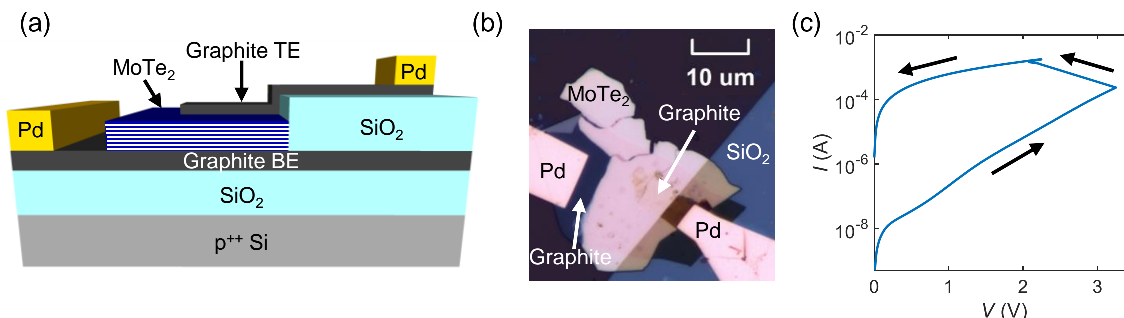


Figure S9. (a) Schematic and (b) optical image of a graphite-$MoTe_2$-graphite device with Pd contacts to the graphite (Device 6). (c) Measured *I-V* curve showing device forming at ~3.2 V, with an external series resistance of 1 kΩ.

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