A COMPACT THERMAL MODEL FOR SEGMENTED NANOWIRE PHASE-CHANGE MEMORY CELLS

By

I-ru Chen

ECE 497/499, Senior Thesis

FALL 2008

Advisor: Professor Eric Pop

December 19, 2008

ABSTRACT

Phase-change memory (PCM) is a promising candidate for next-generation nonvolatile data storage. However, reducing power consumption for PCM cells remains a key challenge, and optimization of write current/power requires a more complete understanding and modeling of the temperature dependence on cell geometry and material properties. Here, a compact model is introduced to show the temperature distribution in cylindrical nanowire phase-change memory (PCM) cells for both transient (~nanosecond) and steady-state time scales. The model takes advantage of the symmetry of the cell to efficiently calculate temperature distribution dependence on geometry and material/interface properties. The results are compared with data from the literature and with finite-element simulations, showing improved computation speed by up to two orders of magnitude. Programming current sensitivity to cell dimensions and material properties is investigated, indicating that nanowire diameter and thermal boundary resistance play the strongest role in enhancing PCM energy efficiency. The model proposed here enables the efficient simulation of PCM cell arrays using circuit simulators such as SPICE.

TABLE OF CONTENTS

1. INTRODUCTION

1.1. Phase-Change Memory and Phase-Change Materials

The principle of utilizing resistance contrast of chalcogenide materials in memory devices was demonstrated by Ovshinsky in the 1960s [1]. However, no practical applications existed until the discovery of fast crystallizing phase-change materials in the 1990s [2]. As the scaling of flash memory devices slows down, the renewed interest in phase change memory (PCM) devices indicates a promising next-generation nonvolatile memory technology that may eventually replace the mainstream Flash technology. When compared to conventional Flash memory, PCM offers good cycling endurance, extended scalability, and reduced programming and access times [3-5]. Nevertheless, reducing power consumption in PCM cells remains a key challenge, in particular due to the high current (0.5-1 mA) presently required for the crystalline to amorphous phase transition (RESET).

Phase-change materials such as $Ge_2Sb_2Te_5$ (GST) and GeTe are chalcogenide glasses that can reversibly switch between their crystalline and amorphous phase through Joule heating [2]. The resulting resistivity change between the two states is more than 100x (Figure 1); thus, stored information can be easily retrieved by measuring the readout current during the application of a small voltage. Substantial readout current implies the GST layer at its crystalline state; similarly, nearly zero readout current is observed when the GST layer is at its amorphous state.

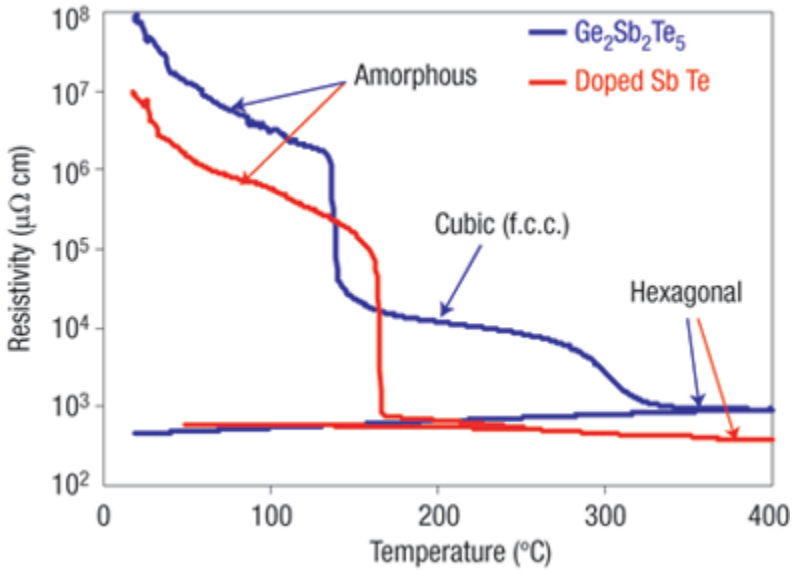

Figure 1. Temperature dependence of chalcogenide resistivity [6].

I-V and memory switching characteristics of a typical PCM cell are shown in Figure 2. Nanosecond programming time and low programming voltage are observed in PCM due to remarkable crystallization kinetics and threshold switching behavior exhibited by GST [7, 8]. The amorphous to crystalline phase transition (SET) requires the GST material to be heated up to its crystallization temperature (~150 ˚C). The GST layer must maintain at this temperature for more than ~100 ns for crystallization to occur (Figure 2b). The RESET operation requires the GST material to be heated up to its melting temperature (~ 600 ˚C). Therefore, RESET current has been the factor that dominates the power consumption of PCM cells, while the required pulse width for SET current has been the factor that limits the speed of PCM devices [3]. Lowering the programming current would also downsize the PCM access transistors, enabling higher bit density. To optimize PCM programming current and energy efficiency, a complete understanding and modeling of the temperature distribution in PCM cells is required.

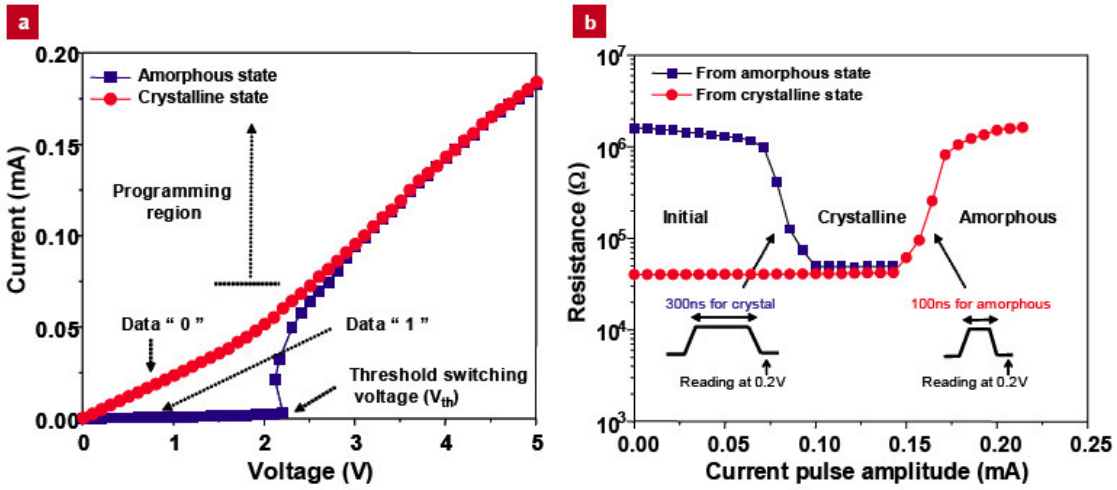

Figure 2. Characteristics of a typical PCM cell with GST as the phase-change material [9]. (a) I-V characteristics with GST in both amorphous and crystalline states. Threshold switching voltage is indicated on the amorphous curve. (b) R-I characteristics and pulse width illustration of the SET and RESET current.

1.2. Segmented Nanowire Phase-Change Memory Cell

Several cell structures have been proposed for PCM devices. Among them, the planar cell structure (Figure 3) is the easiest to fabricate. However, the planar structure requires high programming current and power. Studies have shown that confined PCM cells effectively reduce the programming current while maintaining simple manufacturing steps [10-12]. Figure 4 shows the schematic of a segmented nanowire PCM (NW-PCM) cell. This axisymmetric structure exhibits the best thermal confinement and is the ultimately desired cell structure.

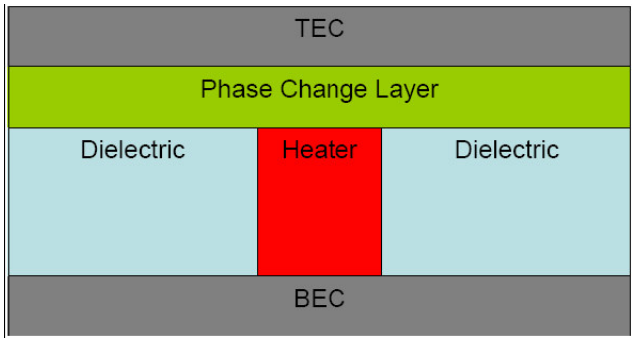

Figure 3. Schematic of a conventional planar PCM cell. Current travels through bottom electrode contact (BEC), heater, phase change (GST) layer, and top electrode contact (TEC) to induce phase transitions.

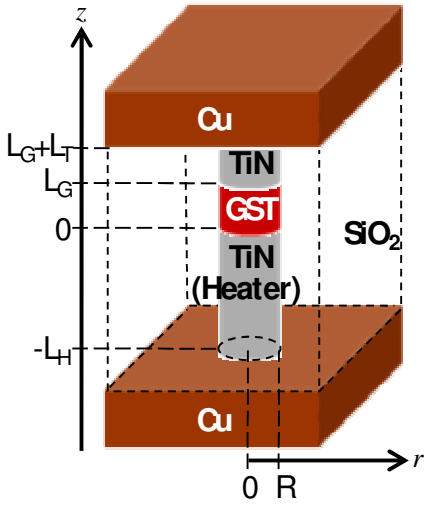

Figure 4. Schematic of a segmented nanowire PCM cell. GST, TiN, SiO_2 and copper serves as the phase-change layer, the electrodes, the interlayer dielectrics, and the electrode contacts, respectively. Geometric parameters used in later simulations are labeled on axes.

2. LITERATURE REVIEW

2.1. Previous Work

Previous modeling work has focused on finite-element (FE) simulations for PCM cells [5, 13]. Reifenberg et al. explored the effects of thermal boundary resistance (TBR) with FE models and showed a 20-30% reduction in programming current for a TBR of 50×10^{-9} m^2K/W [14]. However, FE simulations are time-consuming and not suited for circuit analysis. Simple analytic models have been proposed using circuit equivalents [15], yet these models are too simple to make accurate predictions, particularly in transient time steps. Most recently, Reifenberg et al. modeled the steady-state temperature distribution in PCM cells using the thermal fin model analysis [10]. These analytic models offer limited insight into the geometric dependence of PCM programming current, but the transient temperature distribution in PCM cells remains unsolved.

Several experimental studies have demonstrated relatively low programming current for PCM cells. One of the most popular techniques is to confine the GST layer to a small nanopore, as shown in Figure 5a. Samsung Electronics has successfully fabricated confined PCM cells that are highly scalable and compatible with current CMOS technology [12]. Chao et al. improved this technique by adding an extra GST layer under the pore to suppress the thermal leakage [11]. The result showed ~50% reduction in programming current when compared with planar structure. Another novel concept to reduce the programming current is using GST nanowires as the phase-change layer [6, 9]. Under this concept, Lankhorst et al. proposed a line cell structure using doped SbTe nanowire (Figure 5b) [6]. Nevertheless, more modeling studies for these experimental works are required for PCM to realize its potential.

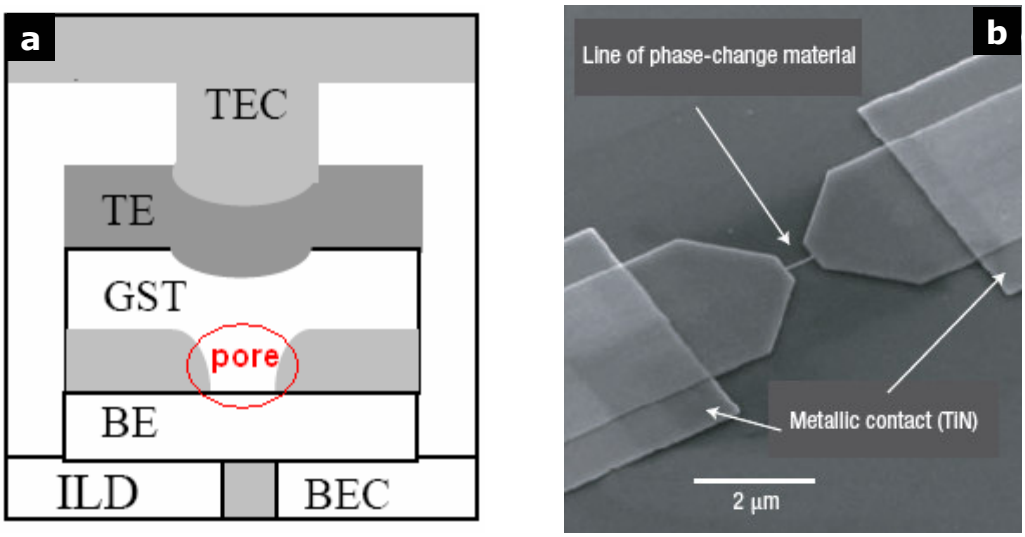

Figure 5. (a) General schematic of confined nanopore structure for PCM cells [12]. (b) SEM image of the line cell structure with GST nanowire and TiN contacts [6].

2.2. Thesis Scope

This work introduces an efficient compact thermal model which yields both the time- and position-dependent temperature distribution during RESET operation in segmented NW-PCM cells. Temperature distribution in both transient and steady-state time scales will be computed self-consistently with the thermal and electrical behaviors. The distribution is obtained by solving the heat diffusion equation, including effects of TBR, and taking advantage of the cylindrical cell symmetry in segmented NW-PCM cells (Figure 4). The compact model is benchmarked with FE simulations in both steady-state and transient (nanosecond time scale) conditions to ensure the validity of the model. The applicability of the model is verified by adjusting different variables, including the aspect ratio of PCM cells, length of the GST/TiN layers, material properties, and values for TBR. Finally, the programming current dependence on cell geometry, material properties and TBR is explored. The results are compared with data available in the literature.

3. FINITE ELEMENT MODEL

3.1. Heat Diffusion Equation with Cylindrical Symmetry

The governing law of heat conduction is the heat diffusion equation with internal heat generation:

$$\nabla^2 T + \frac{Q'''}{k} = \frac{C}{k}\frac{\partial T}{\partial t}, \tag{1}$$

where T is the temperature rise above ambient, k is the thermal conductivity, and C is the volumetric heat capacity. The heat generation rate per unit volume $Q''' = \rho I^2 / A^2$ is limited to the nanowire regions (GST and TiN), where I is the current passing through NW and $A = \pi R^2$ is the cross-sectional area.

The segmented NW-PCM cell in Figure 4 exhibits perfect cylindrical symmetry around the $r = 0$ axis. Therefore, Equation (1) can be simplified by taking advantage of this symmetry:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T}{\partial r}\right) + \frac{\partial T^2}{\partial z^2} + \frac{Q'''}{k} = \frac{C}{k}\frac{\partial T}{\partial t}. \tag{2}$$

The geometric parameters of a segmented NW-PCM cell are labeled in Figure 4, and the default material properties used in the simulation are listed in Table 1. These include the electrical resistivity ρ, thermal conductivity k, and volumetric heat capacity C. The thermal diffusivity is $\alpha = k/C$. Equation (2) can be numerically solved by converting it to a 2-D partial differential equation. The symmetric axis ($r = 0$) is set as the adiabatic boundary ($dT/dr = 0$) and the boundaries sufficiently far away from the nanowire in both radial and axial directions are set as isothermal ($T = 0$).

TABLE 1. MATERIAL AND INTERFACE PROPERTIES USED IN SIMULATIONS

	k (W/m-K)	C (J/cm^3-K)
GST	1.5 (crystalline) 0.25 (amorphous)	1.239
TiN	9.0	4.212
SiO_2	1.3	2.200
Cu	100	3.382
TBR (R_B)	25×10^{-9} m^{2}K/W	
ρ_{TiN}	2.9×10^{-5} Ω-m	
ρ_{GST}	1×10^{-5} Ω-m (hcp) 10×10^{-5} Ω-m (fcc)	

3.2. Thermal Boundaries

Thermal boundary resistance is modeled at the oxide-NW and GST-TiN interfaces and the temperature dependence of TBR is neglected [14]. In FE model simulations, the thermal boundaries are modeled by adding thin boundary layers between bulk materials. The effective thermal conductivity of the thin layers is d / R_B, where d is the thickness of the boundary layer and R_B is the TBR. Other material properties remain the same as the bulk material.

3.3. Simulation Result

The simulation result is shown in Figure 6. The geometric parameters used in the simulation are: R = 20 nm, L_T = 20 nm, L_G = 20 nm, L_H = 100 nm. Note that the temperature in the GST layer (0 nm < z < 20 nm, 0 nm < r < 20 nm) is higher than 600 K, which induces the RESET transition. Material properties are based on Table 1, with GST resis-

tivity using that of the hexagonal close packed structure (hcp). For this particular geometry, the simulation takes 38.3 s and is clearly unacceptable for simulating PCM cell arrays. Nevertheless, FE model results can be used to verify the analytic results.

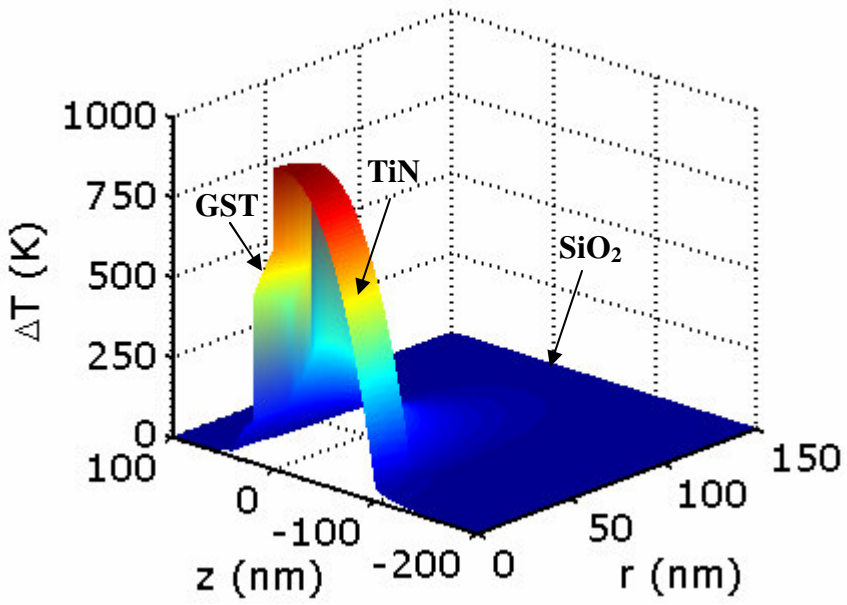

Figure 6. Steady-state temperature distribution obtained using FE model simulation.

4. COMPACT THERMAL MODEL

The compact thermal model focuses on analytically solving Equation (2) with logical approximations. To simplify the calculation, heating in the three confined regions can be analyzed separately and then superposed to form the overall temperature distribution:

$$\Delta T(r,z,t) = T_H(r,z,t) + T_T(r,z,t) + T_G(r,z,t), \tag{3}$$

where $T_H(r,z,t)$, $T_T(r,z,t)$, $T_G(r,z,t)$ are the temperature distribution resulted from heating in TiN heater, top TiN layer, and GST layer, respectively. In this chapter the derivation for $T_H(r,z,t)$ and $T_G(r,z,t)$ will be discussed.

4.1. TiN Heating

First, we consider the heating in the bottom TiN heater alone (T_H). Note that the heating in the top TiN electrode (T_T) can be treated identically. Given the narrow diameter, surrounding TBR, and high k_{TiN}, the lateral temperature may be assumed uniform in the NW, but decays exponentially in SiO_2 with $\exp\left(-r^2/4\alpha_{SiO_2}t\right)/r$ dependence. This is supported by FE simulations, allowing us to eliminate the radial term of Equation (2):

$$\frac{\partial T^2}{\partial z^2} + \frac{Q'''}{k} = \frac{C}{k}\frac{\partial T}{\partial t}. \tag{4}$$

The steady-state solution can be approximated as quadratic in the heater along the z-axis, where $Q''' = \rho_{TiN} I^2 / A^2$, and as linear in the GST, where $Q''' = 0$. The transient solution is obtained by energy conservation arguments and described in more detail further below. The Cu interconnect and top TiN regions are modeled as isothermal (T = 0) by observing FE model results. The temperature distribution is then:

$$T_H(r,z,t)=\begin{cases} T_H^{hot}\left[1-\left(\dfrac{Z_H+z}{Z_H-L_H}\right)^2\right] & ,-L_H<z<0 \text{ and } 0<r<R \\ T_1+\dfrac{z}{L_G}(T_2-T_1) & ,0<z<L_G \text{ and } 0<r<R \\ T_H(R^+,z,t)\exp\left(-\dfrac{r^2-R^2}{4\alpha_{SiO_2}t}\right)\dfrac{R}{r} & ,r>R \end{cases}, \quad (5)$$

where Z_H is the peak temperature location in the heater and $T_H^{hot}(t)=T_H(0,-Z_H,t)$ is the peak temperature in the TiN heater; $T_1(t)=T_H(0,0^+,t)$ and $T_2(t)=T_H(0,L_G^-,t)$ are temperatures in the GST at its bottom and top interfaces, respectively. These temperatures can be obtained by balancing the heat flux across material boundaries:

$$\frac{T_H(0,0^-,t)-T_H(0,0^+,t)}{R_B^{GST-TiN}}=-k_{TiN}\left.\frac{\partial T_H(0,z,t)}{\partial z}\right|_{z=0^-}=-k_{GST}\left.\frac{\partial T_H(0,z,t)}{\partial z}\right|_{z=0^+} \quad (6)$$

$$\frac{T_H(0,L_G^-,t)-T_H(0,L_G^+,t)}{aR_B^{GST-TiN}}=-k_{GST}\left.\frac{\partial T_H(0,z,t)}{\partial z}\right|_{z=L_G^-} \quad (7)$$

$$\frac{T_H(R^-,z,t)-T_H(R^+,z,t)}{R_B^{SiO_2-GST/TiN}}=-k_{SiO_2}\left.\frac{\partial T_H}{\partial r}\right|_{r=R^+} \quad (8)$$

where R_B represents the TBR at boundaries and the parameter a ($0 < a < 1$) accounts for the spreading lateral heat loss from the TiN heater segment to Cu interconnect through the oxide. This parameter is empirically related to the aspect ratio of the NW cell, $AR = (L_T+L_G+L_H)/D$, and the relation of $a = 1.4/AR$ is found to provide the best agreement with FE simulations. Equations (6)-(8) obey the heat conduction law at $z = 0$ (GST-heater interface), $z = L_G$ (GST-top TiN interface), and $r = R$ (oxide-NW interface), respectively.

From equations (5)-(8), the location of the peak temperature in the heater (Z_H) can be obtained, and $T_H(r,z,t)$ is expressed as a function of $T_H^{hot}(t)$ alone. Furthermore, energy conservation must be satisfied as the heat diffuses out at arbitrary transient time t:

$$I^2 \frac{\rho_{TiN} L_H}{A} t = E_G(t) + bE_H(t) + E_{ox}^{diff}(t) + E_{TCu}^{diff}(t) + E_{BCu}^{diff}(t). \quad (9)$$

The first two terms on the right hand side account for the energy to heat up the NW:

$$\begin{cases} E_G(t) = A\int_0^{L_G} C_{GST} T_H(0,z,t)dz \\ E_H(t) = A\int_{-L_H}^{0} C_{TiN} T_H(0,z,t)dz \end{cases}. \quad (10)$$

These terms are significant at transient (~nanosecond) time scales, requiring a parameter b ($1 < b < 2$) to account for the initial heating in TiN. $b = 1.5$ is found to provide the best match with FE simulations, and is used throughout the rest of our modeled results. The latter three terms in Equation (9) account for the energy diffused outside the NW: $E_{ox}^{diff}(t)$ is the energy lost through the entire NW-oxide interface, $E_{TCu}^{diff}(t)$ denotes energy lost from GST to the top Cu interconnect, and $E_{BCu}^{diff}(t)$ denotes energy similarly lost from heater to bottom Cu interconnect. These terms are more significant when the temperature distribution in the cell reaches steady-state. The total energy lost from the NW can be calculated by integrating over time, at interfaces:

$$\begin{cases} E_{ox}^{diff}(t) = \int_0^t 2\pi R\int_{-L_H}^{L_G} -k_{SiO_2} \left.\frac{\partial T_H(r,z,\tau)}{\partial r}\right|_{r=R^+} dz d\tau \\ E_{TCu}^{diff}(t) = A\int_0^t -k_{GST} \left.\frac{\partial T_H(0,z,\tau)}{\partial z}\right|_{z=L_G^-} d\tau \\ E_{BCu}^{diff}(t) = A\int_0^t k_{TiN} \left.\frac{\partial T_H(0,z,\tau)}{\partial z}\right|_{z=-L_H^+} d\tau \end{cases}. \quad (11)$$

$T_H^{hot}(t)$ as a function of time is obtained analytically by substituting Equations (10) and (11) into Equation (9). The time- and position-dependent temperature distribution $T_H(r,z,t)$ can be derived from $T_H^{hot}(t)$ using the calculated relationship from Equations (5)-(8).

4.2. GST Heating

The next step considers heating in the GST region alone. Similar to the analysis above, the axial temperature distribution is quadratic in the heated GST region, where $Q'''= \rho_{GST} I^2 / A^2$, and is linear in the unheated TiN regions. Closely following the analysis in Section 4.1, the axial distribution from GST heating can be expressed as:

$$T_G(0,z,t)=\begin{cases} T_G^{hot}+\left(T_3-T_G^{hot}\right)\left(\dfrac{z-Z_G}{Z_G}\right)^2 & ,\ 0<z<L_G \\ T_G\left(0,L_G{}^{+},t\right)\times\dfrac{L_G+L_T-z}{L_T} & ,\ L_G<z<L_G+L_T\ , \\ T_G\left(0,0^{-},t\right)\times\dfrac{L_H+z}{L_H} & ,\ -L_H<z<0 \end{cases} \tag{12}$$

where $(r,z)=(0,Z_G)$ is the peak temperature location in the GST, $T_G^{hot}(t)=T_G(0,Z_G,t)$, and $T_3(t)=T_G\left(0,0^{+},t\right)$. Again, the heat flux across GST-TiN interfaces must be balanced:

$$\frac{T_G\left(0,0^{-},t\right)-T_G\left(0,0^{+},t\right)}{R_B^{GST-TiN}}=-k_{TiN}\left.\frac{\partial T_G(0,z,t)}{\partial z}\right|_{z=0^{-}}=-k_{GST}\left.\frac{\partial T_G(0,z,t)}{\partial z}\right|_{z=0^{+}}, \tag{13}$$

$$\frac{T_G\left(0,L_G{}^{-},t\right)-T_G\left(0,L_G{}^{+},t\right)}{R_B^{GST-TiN}}=-k_{GST}\left.\frac{\partial T_G(0,z,t)}{\partial z}\right|_{z=L_G{}^{-}}=-k_{TiN}\left.\frac{\partial T_G(0,z,t)}{\partial z}\right|_{z=L_G{}^{+}}. \tag{14}$$

Equations (13) and (14) follow the heat conduction law at z = 0 (GST-heater interface) and $z = L_G$ (GST-top TiN interface), respectively. Replacing T_G in (13) and (14) with the T_G specified in (12), Z_G can be obtained and $T_G(0,z,t)$ can be explicitly expressed in terms of $T_G^{hot}(t)$. However, the lateral temperature cannot be assumed as uniform within the GST, as the thermal conductivity of GST is comparable to that of the surrounding SiO_2. The radial temperature is modeled as quadratic:

$$T_G(r,z,t)=\begin{cases} T_G(0,z,t)+\left(T_G(R^-,z,t)-T_G(0,z,t)\right)\left(\dfrac{r}{R}\right)^2 & , r<R \\ T_G(R^+,z,t)\exp\left(-\dfrac{r^2-R^2}{4\alpha_{SiO_2}t}\right)\dfrac{R}{r} & , r>R \end{cases}, \quad (15)$$

with the boundary condition at $r = R$:

$$\frac{T_G(R^-,z,t)-T_G(R^+,z,t)}{R_B^{SiO_2-GST/TiN}}=-k_{GST/TiN}\left.\frac{\partial T_G}{\partial r}\right|_{r=R^-}=-k_{SiO_2}\left.\frac{\partial T_G}{\partial r}\right|_{r=R^+}. \quad (16)$$

$T_G(r,z,t)$ can be expressed in terms of $T_G^{hot}(t)$ by substituting Equation (15) into Equation (16) and using results from Equations (12)-(14). $T_G^{hot}(t)$ is then explicitly solved by taking advantage of the energy conservation law:

$$I^2\frac{\rho_{GST}L_G}{A}t=E_G(t)+\frac{E_H(t)+E_T(t)}{b}+cE_{ox}^{diff}(t)+E_{TCu}^{diff}(t)+E_{BCu}^{diff}(t), \quad (17)$$

where b accounts for the initial heating in TiN as in Equation (9), and c is an empirical parameter which accounts for spreading lateral heat loss from the NW to the Cu interconnect through the oxide ($c = 5L_G/(L_T + L_H - 0.25L_G)$).

Similar to Equation (10), the first three terms are more significant at transient time steps and account for the energy used to increase the temperature in NW. Unlike Equation (9), $E_H(t)$ and $E_T(t)$ in Equation (17) denote the energy diffused from the GST layer to TiN regions, and therefore $E_H(t)$ and $E_T(t)$ are divided by b. The latter three terms account for the energy diffused out of the nanowire and are more significant when the system reaches steady-state. The six terms on the right hand side of Equation (17) are calculated as:

$$\begin{cases} E_G(t) = \int_0^R \int_0^{L_G} C_{GST} T_G(r,z,t) \times 2\pi r dz dr \\ E_H(t) = \int_0^R \int_{-L_H}^0 C_{TiN} T_G(r,z,t) \times 2\pi r dz dr \\ E_T(t) = \int_0^R \int_{L_G}^{L_G+L_T} C_{TiN} T_G(r,z,t) \times 2\pi r dz dr \end{cases}, \tag{18}$$

$$\begin{cases} E_{ox}^{diff}(t) = \int_0^t 2\pi R \int_{-L_H}^{L_G} -k_{SiO_2} \left.\frac{\partial T_G(r,z,\tau)}{\partial r}\right|_{r=R^+} dz d\tau \\ E_{TCu}^{diff}(t) = \int_0^R \int_0^t -k_{TiN} \left.\frac{\partial T_G(r,z,\tau)}{\partial z}\right|_{z=(L_G+L_T)^-} 2\pi r d\tau dr \\ E_{BCu}^{diff}(t) = \int_0^R \int_0^t k_{TiN} \left.\frac{\partial T_G(r,z,\tau)}{\partial z}\right|_{z=-L_H^+} 2\pi r d\tau dr \end{cases}. \tag{19}$$

4.3. Results and Discussion

As shown in Equation (3), the total temperature solution is finally obtained by superposing the heating from bottom electrode $T_H(r,z,t)$, top electrode $T_T(r,z,t)$, and GST layer $T_G(r,z,t)$. The results of this model with default parameters (Table 1) are shown in Figures 7-9, and compared with comprehensive FE simulations. In these figures, simulations are run with diameter D = 40 nm, segment lengths L_H = 100 nm (bottom TiN heater), L_G = 20 nm (GST) and L_T = 20 nm (top TiN). Symbols represent FE model simulation results, and lines are compact model results. Note that the analytic model provides the correct temperature dependence in both temporal and spatial variations. The agreement with FE simulations is better than 10% at the key temperature points, and correctly reproduces the temperature drops at boundaries due to TBR. In addition, the simulation time is reduced by approximately two orders of magnitude, enabling a novel and robust approach for circuit simulation of entire PCM cell arrays.

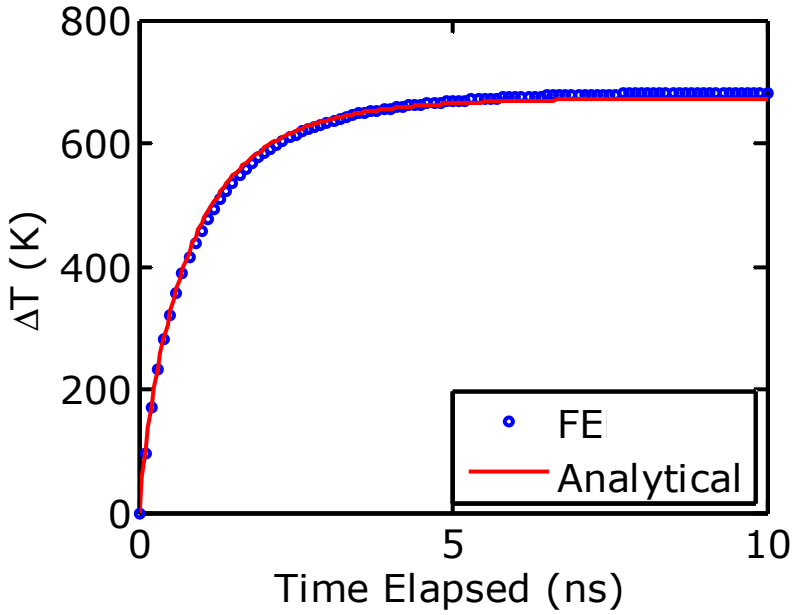

Figure 7. Transient temperature profile at the hot point in GST.

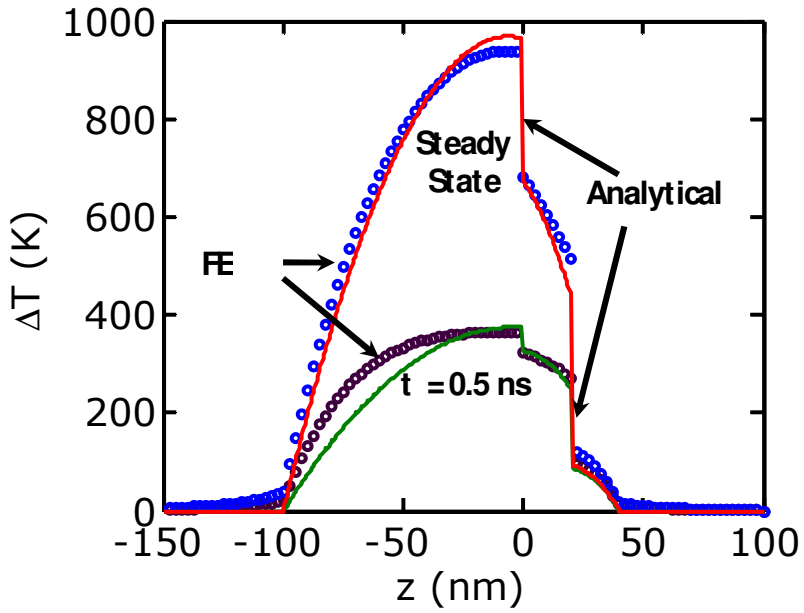

Figure 8. Axial temperature profile, along the axis of symmetry ($r = 0$) at transient time $t = 0.5$ ns, and after steady-state is reached. Transient analytical result slightly deviates from FE model simulation in heater region, but agreed nearly perfectly in active GST region.

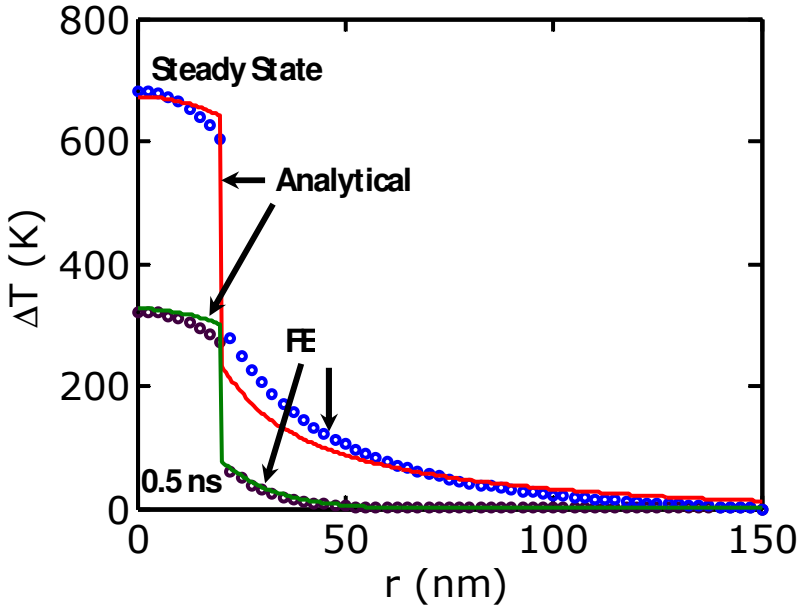

Figure 9. Radial temperature profile at the GST-heater interface ($z = 0^+$).

5. SENSITIVITY ANALYSIS

Based on the efficient thermal model described above, the minimum programming current for the GST layer to reach melting temperature (ΔT ~ 600 K) can be obtained by providing geometric parameters, material properties, and TBRs. The results are collected and shown in this chapter for typical ranges of cell geometry and material properties. Once again, these results are compared with FE simulations, finding agreement within 10%.

5.1. Sensitivity to Cell Geometry

Figure 10 displays the expected correlation between NW diameter and programming current. Solid lines show the case when the total NW length ($L_{NW} = L_T+L_G+L_H$) is fixed and when the cell resistance is proportional to $1/D^2$. Dashed lines show the case when the aspect ratio (AR) of cell segments is fixed, but L_{NW} is varied. In this case the cell resistance is proportional to $1/D$. Blue, red and black dashed lines are for AR = 3, 4, and 5, respectively. As shown in Figure 10, stronger diameter dependence is observed when L_{NW} is fixed. For the total programming power shown in the inset, this stronger dependence is cancelled by the inverse relationship with the electrical cell resistance, and all curves fall roughly on the same trend. Although our default material parameter set is somewhat generic, and not fit to any particular test structure, the confined GST pore cell demonstrates a very similar trend to our model when L_{NW} is fixed [11]. In practice, as with any physically-based compact model, the exact material parameters must be treated as adjustable inputs, and fit to the empirical data.

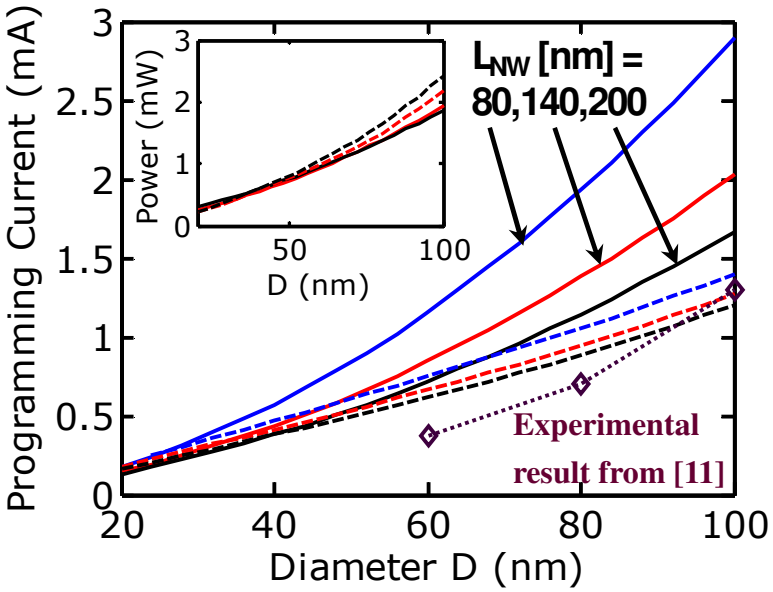

Figure 10. Diameter dependence of the programming current.

Extending the bottom heater length L_H can reduce the programming current as more energy is transferred to and kept in the GST layer. However, this is only effective up to a point, as shown in Figure 11. Extending L_H beyond the "knee" indicated by vertical dashes simply causes additional energy to diffuse laterally out of the NW without efficiently heating the GST layer.

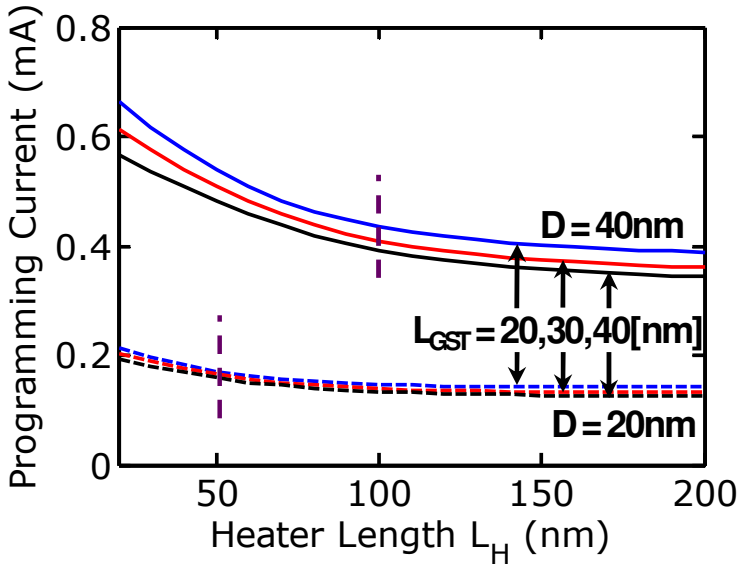

Figure 11. Heater length dependence of the programming current, for two diameters.

Figure 12 shows the interesting result of varying only the heater-GST ratio, with the top electrode length fixed at L_T = 10 nm. A minimum programming current is expected when the ratio L_H / L_G ≈ 2–4, but a longer NW (L_{NW}) eventually increases cell resistance and reduces the programming current. Thus, an optimum heater-GST aspect ratio is expected for a given top electrode thickness, cell diameter, and material property set.

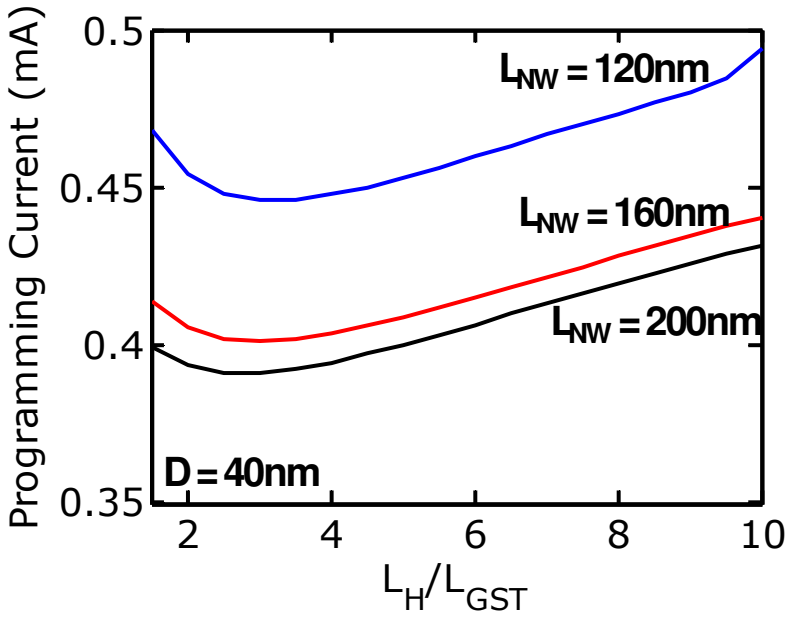

Figure 12. Programming current as a function of the heater-GST ratio.

5.2. Sensitivity to Material and Interface Properties

Before concluding, the model sensitivity to material and interface properties is explored. These properties may be varied in practice by altering GST stoichiometry [16], replacing SiO_2 with other insulators, or changing the heater material. As shown in Figure 13, lowering thermal conductivity of all materials typically leads to better thermal confinement and reduced programming current. Variations in temperature may also affect the thermal conductivity, although this is more pronounced in crystalline materials below their Debye temperature (e.g. silicon, SiC, AlN, or carbon nanotubes). This is not the

typical case for PCM, with amorphous or polycrystalline materials operating in the range 300-900 K, or above their Debye temperature.

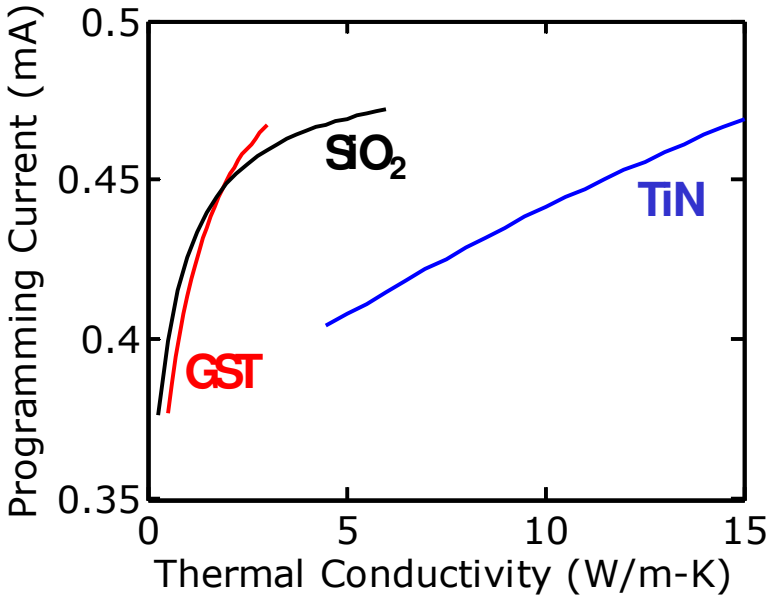

Figure 13. Dependence of the programming current on typical ranges of material thermal conductivity. Geometric parameters are R = 20 nm, $L_T = L_G$ = 20 nm and L_H = 100 nm.

Finally, the role of thermal boundary resistance (TBR) and GST resistivity is examined in Figure 14. The TBR for most phase-change materials is expected to fall approximately in the range of 0–100 m^2K/GW [14]. Higher TBR is typically desired in PCM, giving better thermal confinement and lower programming current. Note that the model predicts the most significant impact from increased TBR (up to 3x lower RESET current) and smaller diameter, versus changes in other material parameters within their reasonably expected ranges. A reduced programming current is also observed by increasing the GST resistivity, where the electron contribution to GST thermal conductivity is correlated through the Wiedemann-Franz Lorenz Law.

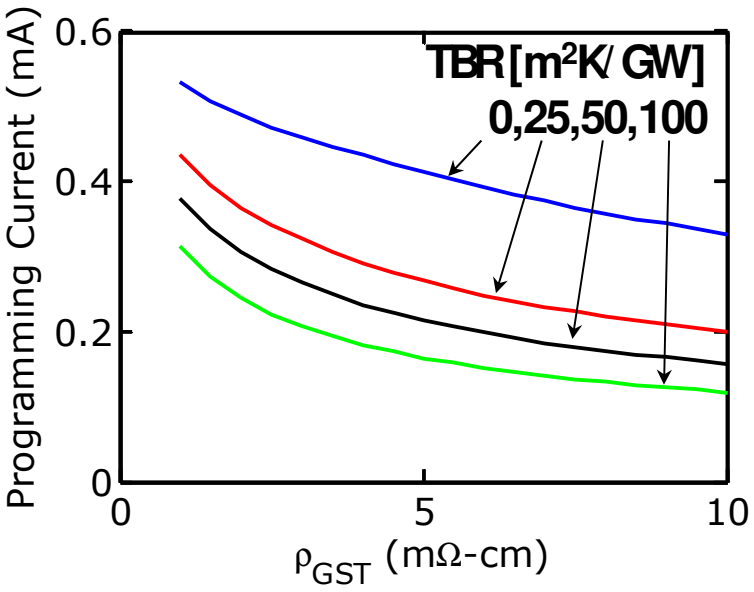

Figure 14. Dependence of programming current on TBR and GST resistivity reveals a strongest dependence on the former.

6. CONCLUSION

In summary, an efficient compact thermal model is introduced to analyze the temperature distribution in segmented nanowire PCM cells, in both transient and steady-state time scales. The model is derived by solving the heat diffusion equation, including effects of thermal boundary resistance, and taking advantage of the cylindrical cell symmetry. The results agree with FE simulations within 10% error, at up to two orders of magnitude reduced computational time. The analytic solution offers physical insights into energy diffusion across materials and boundaries, and allows us to quickly optimize the programming current with respect to cell geometry, material properties and TBR. The model proposed here will also enable the efficient treatment of PCM cell arrays within circuit simulators such as SPICE.

The future work of this project involves including the electrical behaviors as well as the melting and crystallization dynamics into the model. The self-consistent single-cell model will be extended to cell arrays. Thermal crosstalk between cells will be incorporated by adjusting the single-cell model. The adjusted model will be run in parallel to study the effect of high-temperature write operations. In particular, the effect of RESET operation will receive special attention since the high temperature required in the process may cause unwanted crystallization and threaten the data if the GST layers in adjacent cells are amorphous. The data retention lifetime will be calculated from the simulation data and be compared with that extrapolated from Arrhenius law.

REFERENCES

[1] S. R. Ovshinsky, "Reversible electrical switching phenomena in disorder structures," *Phys. Rev. Lett.,* vol. 21, pp. 1450-1453, 1968.

[2] N. Yamada, E. Ohno, K. Nishiuchi, and N. Akahira, "Rapid-phase transitions of GeTe-Sb_2Te_3 pseudobinary amorphous thin films for an optical disk memory," *J. Appl. Phys,* vol. 69, pp. 2849-2856, 1991.

[3] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y.-C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S.-H. Chen, H.-L. Lung, and C. H. Lam, "Phase-change random access memory: A scalable technology," *IBM J. Res. & Dev.,* vol. 52, pp. 465-479, 2008.

[4] A. L. Lacaita, "Phase-change memory: State-of-art, challenges, and perspectives," *Solid-state Electronics,* vol. 50, pp. 24-31, 2006.

[5] A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, "Scaling analysis of phase-change memory technology," in *IEDM Tech. Dig.*, 2003, pp. 699-702.

[6] M. Lankhorst, B. Ketelaars, and R. Wolters, "Low-cost and nanoscale non-volatile memory concept for future silicon chips," *Nature Materials,* vol. 4, pp. 347-352, 2005.

[7] M. Wuttig and N. Yamada, "Phase-change materials for rewriteable data storage," *Nature Materials,* vol. 6, pp. 824-832, 2007.

[8] A. Redaelli, A. Pirovano, F. Pellizzer, A. L. Lacaita, D. Ielmini, and R. Bez, "Electronic switching effect and phase-change transition in chalcogenide materials," *IEEE Elec. Dev. Lett.,* vol. 25, pp. 684-686, 2004.

[9] S.-H. Lee, Y. Jung, and R. Agarwal, "Highly scalable non-volatile and ultra-low-power phase-change nanowire memory," *Nature Nanotechnology,* vol. 2, pp. 626-630, 2007.

[10] J. P. Reifenberg, H. Gupta, M. Asheghi, and K. E. Goodson, "Closed form thermal analysis of phase change memory devices," in *ECI Intl. Conf. on Heat Transfer and Fluid Flow in Microscales*, Whistler, BC, Canada, 2008.

[11] D.-S. Chao, Y.-C. Chen, F. Chen, M.-J. Chen, P. H. Yen, C.-M. Lee, W.-S. Chen, C. Lien, M.-J. Kao, and M.-J. Tsai, "Enhanced thermal efficiency in phase-change memory cell by double GST thermally confined structure," *IEEE Elec. Dev. Lett.,* vol. 28, pp. 871-873, 2007.

[12] S. L. Cho, J. H. Yi, Y. H. Ha, B. J. Kuh, C. M. Lee, J. H. Park, S. D. Nam, H. Horii, B. O. Cho, K. C. Ryoo, S. O. Park, H. S. Kim, U.-I. Chung, J. T. Moon, and B. I. Ryu, "Highly scalable on-axis confined cell structure for high density PRAM beyond 256MB," in *Symp. VLSI Tech. Dig.*, 2005.

[13] A. L. Lacaita, A. Redaelli, D. Ielmini, F. Pellizzer, A. Pirovano, A. Benvenuti, and R. Bez, "Electrothermal and phase-change dynamics in chalcogenide-based memories," in *IEDM Tech. Dig.*, 2004, pp. 911-914.

[14] J. P. Reifenberg, D. L. Kencke, and K. E. Goodson, "The impact of thermal boundary resistance in phase-change memory devices," *IEEE Elec. Dev. Lett.,* vol. 29, pp. 1112-1114, 2008.

[15] U. Russo, D. Ielmini, A. Redaelli, and A. L. Lacaita, "Modeling of programming and read performance in phase-change memories—Part I: Cell optimization and scaling," *IEEE Trans. Elec. Dev.,* vol. 55, pp. 506-514, 2008.

[16] J. P. Reifenberg, M. A. Panzer, S. Kim, A. M. Gibby, Y. Zhang, S. Wong, H.-S. P. Wong, E. Pop, and K. E. Goodson, "Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films," *Appl. Phys. Lett.,* vol. 91, p. 111904, 2007.