Compact Thermal Model for Vertical Nanowire Phase-Change Memory Cells

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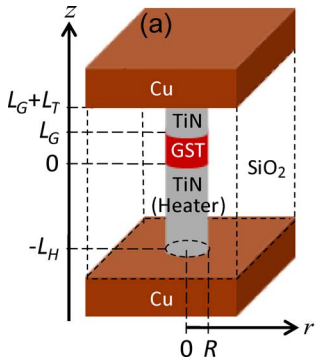
***Abstract*—We introduce a compact model for the temperature distribution in cylindrical nanowire (NW) phase-change memory (PCM) cells for both transient (nanoseconds) and steady-state time scales. The model takes advantage of the symmetry of the cell to efficiently calculate temperature distribution dependence on geometry and material/interface properties. The results are compared with data from the literature and with finite-element simulations, showing improved computation speed by two orders of magnitude. Programming current sensitivity to cell dimensions and material properties is investigated, indicating that NW diameter (D) and thermal boundary resistance (TBR) play the strongest role in enhancing PCM energy efficiency.**

***Index Terms*—Compact model, GST nanowire (NW), phase-change memory (PCM), thermal transport.**

I. Introduction

PHASE-CHANGE memory (PCM) is a promising candidate for next-generation nonvolatile data storage, offering good cycling endurance, extended scalability, and reduced programming/access times [1]–[3]. Phase-change materials such as $Ge_2Sb_2Te_5$ (GST) and GeTe are chalcogenide glasses that can reversibly switch between their crystalline and amorphous phases through Joule heating [4]. A large resistivity change ($> 100\times$) between the two states allows the bit to be stored as 0 or 1, while programming is achieved at nanosecond time scales and low ($\sim$1 V) voltages [5], [6]. Nevertheless, reducing power consumption in PCM cells remains a key challenge, in particular due to the high current ($\sim$0.5 mA) presently required for the crystalline-to-amorphous phase transition (RESET) [1]. Lowering the programming current would also downsize the PCM access transistors, enabling higher bit density. To optimize PCM programming current and energy efficiency, a complete understanding and modeling of the temperature distribution in PCM cells is required.

Previous modeling work has focused on finite-element (FE) simulations for PCM cells [3], [7] and the effect of thermal boundary resistance (TBR) [8]. However, FE simulations are time-consuming and not suited for circuit analysis, while existing analytic models use simple electrical and thermal circuit equivalents [9], [10], offering limited insight into spatial and geometric dependences of the programming current and assuming steady-state operation. An improved analytic model has recently been used to examine the RESET current in a "mushroom" cell [11], yet without including the strong role of TBR. In this brief, we introduce an efficient compact thermal model which yields both time- and position-dependent temperature distributions in PCM cells. We include TBR at material interfaces, and the model enables the calculation of the RESET current and the exact location of the peak temperature in a device without *a priori* assumptions about the latter. In particular, we focus on the nanopore-like [12], [13], [19] or nanowire (NW) [14], [15] device layout, which is thought to exhibit the best thermal confinement, and take advantage of the cylindrical symmetry for efficient modeling. We benchmark our compact model with FE simulations in both steady-state and transient (nanosecond time scale) conditions. Finally, we examine the programming current dependence on cell geometry, material properties, and TBR and compare our results with data available in the literature.



(b)	k (W/m·K)	C (J/cm^3·K)
GST	1.5 (c) 0.25 (a)	1.24
TiN	9.0	4.21
SiO_2	1.3	2.20
TBR	25×10^{-9} m^{2}K/W	
ρ_{TiN}	2.9×10^{-5} Ω·m	
ρ_{GST}	1×10^{-5} Ω·m (hcp) 10×10^{-5} Ω·m (fcc)	

Fig. 1. (a) Schematic of a vertical nanowire PCM cell. (b) Default material and interface properties. These include the electrical resistivity ρ, thermal conductivity k, and heat capacity C. The thermal diffusivity $\alpha = k/C$. Parameter values can be modified or empirically fitted to the particular experimental test structure, materials, and process conditions.

II. Compact Thermal Model

Fig. 1 shows the schematic of a vertical segmented NW PCM cell and the default material properties used in the model. Thermal boundary resistance is a critical component [8], and it is modeled at the oxide–NW and GST–TiN interfaces. The

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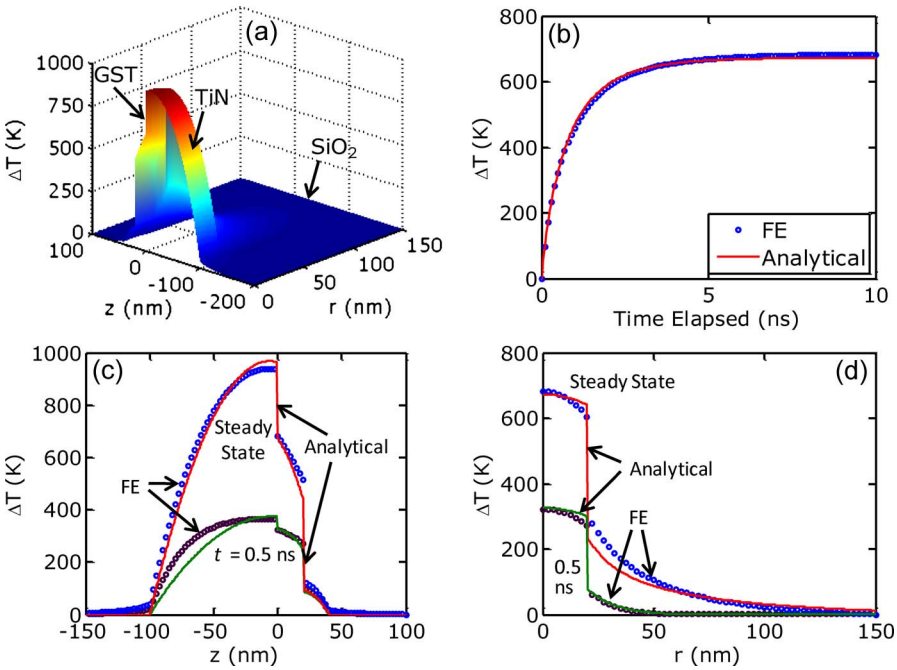

Fig. 2. Comparison between finite-element (FE) and compact model simulations, for PCM cell with diameter $D = 40$ nm, segment lengths $L_H = 100$ nm (bottom TiN heater), $L_G = 20$ nm (GST), and $L_T = 20$ nm (top TiN). Symbols are FE results; lines represent analytic model. (a) Three-dimensional temperature distribution from FE simulation. (b) Transient temperature profile at hot point in GST. (c) Axial temperature profile, along the axis of symmetry ($r = 0$) at transient time $t = 0.5$ ns, and after steady state is reached. (d) Radial temperature profile at GST–heater interface ($z = 0^+$), in the same two time regimes.

transient temperature profiles are obtained from the heat diffusion equation with cylindrical symmetry

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T}{\partial r}\right) + \frac{\partial T^2}{\partial z^2} + \frac{Q'''}{k} = \frac{C}{k}\frac{\partial T}{\partial t} \tag{1}$$

where T is the temperature rise above ambient. The heat generation rate per unit volume $Q''' = \rho(I/A)^2$ is limited to the NW region (GST and TiN), where $A = \pi R^2$ is the cross-sectional area. Heating in the three segment regions can be analyzed separately and then superposed to form the overall temperature distribution. In parallel, we set up a finite-element (FE) simulation of the same test structure to be used for benchmarking and comparison [Fig. 2(a)]. The 3-D heat diffusion equation is reduced to 2-D [see (1)] by taking advantage of the cylindrical symmetry, and the $r = 0$ axis is assumed to be adiabatic. Thermal boundaries are approximated using a very thin layer of material with effective thermal conductivity t_B/R_B, where t_B is the thickness of the boundary layer and R_B is the desired TBR. Boundaries sufficiently far away from the nanowire (i.e., GST and TiN) regions in the $\pm z$- and r-directions are assumed to be isothermal.

First, we consider the case of heating in the bottom TiN heater alone (T_H) and note that heating in the top TiN segment (T_T) can be treated identically. Given the narrow diameter, surrounding TBR, and higher k_{TiN}, we may assume that the lateral temperature is uniform in the NW [10] but decays exponentially in SiO_2 with $\exp(-r^2/4\alpha_{\mathrm{SiO_2}}t)/r$ dependence, where $\alpha_{\mathrm{SiO_2}} = k_{\mathrm{SiO_2}}/C_{\mathrm{SiO_2}}$ is the thermal diffusivity of the oxide, with k and C being the thermal conductivity and volumetric heat capacity, respectively, as shown in Fig. 1(b). This is supported by FE simulations, allowing us to eliminate the radial term of (1) in the NW. The *steady-state* solution can be approximated as quadratic in the heater along the z-axis, where $Q''' = \rho_{\mathrm{TiN}}(I/A)^2$, and as linear in the GST, where $Q''' = 0$.

The *transient* solution is approximated by steady-state solutions with an empirical parameter to account for the initial heating and obtained through energy conservation arguments as further described below. By observing FE model results, we also model the Cu interconnect and top TiN regions to be isothermal ($T = 0$) in this situation. The temperature distribution is then given in (2) shown at the bottom of the page, where Z_H is the peak temperature location in the heater, $T_H^{\mathrm{hot}}(t) = T_H(0, -Z_H, t)$ is the peak temperature, and $T_1(t) = T_H(0, 0^+, t)$ and $T_2(t) = T_H(0, L_G^-, t)$ are temperatures in the GST at its bottom and top interfaces, respectively. The exponential decay into the SiO_2 ($r > R$) is found to be a good analytic description of the temperature evolution by comparison with

$$T_H(r,z,t) = \begin{cases} T_H^{\mathrm{hot}}\left[1 - \left(\frac{Z_H+z}{Z_H-L_H}\right)^2\right], & -L_H < z < 0 \text{ and } 0 < r < R \\ T_1 + \frac{z}{L_G}(T_2 - T_1), & 0 < z < L_G \text{ and } 0 < r < R \\ T_H(R^+, z, t)\exp\left(-\frac{r^2-R^2}{4\alpha_{\mathrm{SiO_2}}t}\right)\frac{R}{r}, & r > R \end{cases} \tag{2}$$

FE simulations [Fig. 2(d)]. Additional relationships are obtained by balancing the heat flux across material boundaries

$$\frac{T_H(0,0^-,t)-T_H(0,0^+,t)}{R_B^{\mathrm{GST-TiN}}} = -k_{\mathrm{TiN}}\frac{\partial T_H(0,z,t)}{\partial z}\bigg|_{z=0^-} = -k_{\mathrm{GST}}\frac{\partial T_H(0,z,t)}{\partial z}\bigg|_{z=0^+} \tag{3}$$

$$\frac{T_H\left(0,L_G^-,t\right)-T_H\left(0,L_G^+,t\right)}{aR_B^{\mathrm{GST-TiN}}} = -k_{\mathrm{GST}}\frac{\partial T_H(0,z,t)}{\partial z}\bigg|_{z=L_G^-} \tag{4}$$

$$\frac{T_H(R^-,z,t)-T_H(R^+,z,t)}{R_B^{\mathrm{SiO_2-GST/TiN}}} = -k_{\mathrm{SiO_2}}\frac{\partial T_H}{\partial r}\bigg|_{r=R^+} \tag{5}$$

where R_B represents the TBR at boundaries and the parameter a $(0<a<1)$ accounts for the spreading lateral heat loss from the GST segment to top Cu interconnect through the oxide, since the top TiN is generally a thin barrier layer between the GST and top Cu regions. We empirically relate this parameter to the aspect ratio (AR) of the NW cell, i.e., $AR=(L_T+L_G+L_H)/D$, and a value $a=1.4/AR$ is found to provide the best agreement with FE simulations. This parameter depends on the AR because for higher ARs, the thermal energy stored in the GST will have more tendency to diffuse laterally, leading to an effectively lower TBR at the top.

From (2)–(5), the location of the peak temperature in the heater (Z_H) can be obtained, and $T_H(r,z,t)$ is expressed as a function of $T_H^{\mathrm{hot}}(t)$ alone. Furthermore, energy conservation must be satisfied as the heat diffuses out at any arbitrary transient time t

$$I^2\frac{\rho_{\mathrm{TiN}}L_H}{A}t = E_G(t)+bE_H(t)+E_{\mathrm{ox}}^{\mathrm{diff}}(t)+E_{\mathrm{TCu}}^{\mathrm{diff}}(t)+E_{\mathrm{BCu}}^{\mathrm{diff}}(t) \tag{6}$$

where the first two terms on the right-hand side account for the energy heating up the GST and TiN heater regions, respectively. $E_G(t)=A\int_0^{L_G}C_{\mathrm{GST}}T_H(0,z,t)dz$ and $E_H(t)$ can be calculated in a similar manner. These terms are significant at transient time scales, requiring a parameter b $(1<b<2)$ to account for the initial heating in TiN. We find that $b=1.5$ provides the best match with FE simulations and use it throughout the rest of our modeled results. The latter three terms in (6) account for the energy diffused outside the NW: $E_{\mathrm{ox}}^{\mathrm{diff}}(t)$ is the energy lost through the entire NW–oxide interface, $E_{\mathrm{TCu}}^{\mathrm{diff}}(t)$ denotes energy lost from GST to the top Cu interconnect, and $E_{\mathrm{BCu}}^{\mathrm{diff}}(t)$ denotes energy similarly lost from heater to the bottom Cu interconnect. These terms are more significant when the temperature distribution in the cell reaches steady state. The total energy lost from the NW can be calculated by integrating over time at interfaces

$$\begin{cases} E_{\mathrm{ox}}^{\mathrm{diff}}(t)=\int_0^t 2\pi R\int_{-L_H}^{L_G}-k_{\mathrm{SiO_2}}\frac{\partial T_H(r,z,\tau)}{\partial r}\Big|_{r=R^+}dzd\tau \\ E_{\mathrm{TCu}}^{\mathrm{diff}}(t)=A\int_0^t -k_{\mathrm{GST}}\frac{\partial T_H(0,z,\tau)}{\partial z}\Big|_{z=L_G^-}d\tau \\ E_{\mathrm{BCu}}^{\mathrm{diff}}(t)=A\int_0^t k_{\mathrm{TiN}}\frac{\partial T_H(0,z,\tau)}{\partial z}\Big|_{z=-L_H^+}d\tau. \end{cases} \tag{7}$$

T_H as a function of time $(T_H^{\mathrm{hot}}(t))$ is obtained analytically by substituting (7) into (6). The time- and position-dependent temperature distribution $T_H(r,z,t)$ can be derived from the calculated $T_H^{\mathrm{hot}}(t)$ above, together with the relationship between $T_H(r,z,t)$ and $T_H^{\mathrm{hot}}(t)$, which is obtained from (2)–(5).

The next step considers heating in the GST region alone. Similar to the earlier discussion, the axial temperature is quadratic in the heated GST region, where $Q'''=\rho_{\mathrm{GST}}(I/A)^2$, and is linear in the unheated TiN regions. Closely following the analysis of (2) for the temperature distribution from TiN heating, the axial distribution from GST heating can be expressed as in (8) shown at the bottom of the page, where Z_G is the peak temperature location in GST, $T_G^{\mathrm{hot}}(t)=T_G(0,Z_G,t)$, and $T_3(t)=T_G(0,0^+,t)$. Again, the heat flux across GST–TiN interfaces must be balanced. By using analysis that is similar to (3) and (4), we balance the heat flux at boundaries

$$\frac{T_G(0,0^-,t)-T_G(0,0^+,t)}{R_B^{\mathrm{GST-TiN}}} = -k_{\mathrm{TiN}}\frac{\partial T_G(0,z,t)}{\partial z}\bigg|_{z=0^-} = -k_{\mathrm{GST}}\frac{\partial T_G(0,z,t)}{\partial z}\bigg|_{z=0^+} \tag{9}$$

$$\frac{T_G\left(0,L_G^-,t\right)-T_G\left(0,L_G^+,t\right)}{R_B^{\mathrm{GST-TiN}}} = -k_{\mathrm{GST}}\frac{\partial T_G(0,z,t)}{\partial z}\bigg|_{z=L_G^-} = -k_{\mathrm{TiN}}\frac{\partial T_G(0,z,t)}{\partial z}\bigg|_{z=L_G^+}. \tag{10}$$

Solving (9) and (10) with the T_G specified in (8), we can obtain Z_G and explicitly express $T_G(0,z,t)$ in terms of $T_G^{\mathrm{hot}}(t)$.

$$T_G(0,z,t)=\begin{cases} T_G^{\mathrm{hot}}+\left(T_3-T_G^{\mathrm{hot}}\right)\left(\frac{z-Z_G}{Z_G}\right)^2, & 0<z<L_G \\ T_G\left(0,L_G^+,t\right)\times\frac{L_G+L_T-z}{L_T}, & L_G<z<L_G+L_T \\ T_G(0,0^-,t)\times\frac{L_H+z}{L_H}, & -L_H<z<0 \end{cases} \tag{8}$$

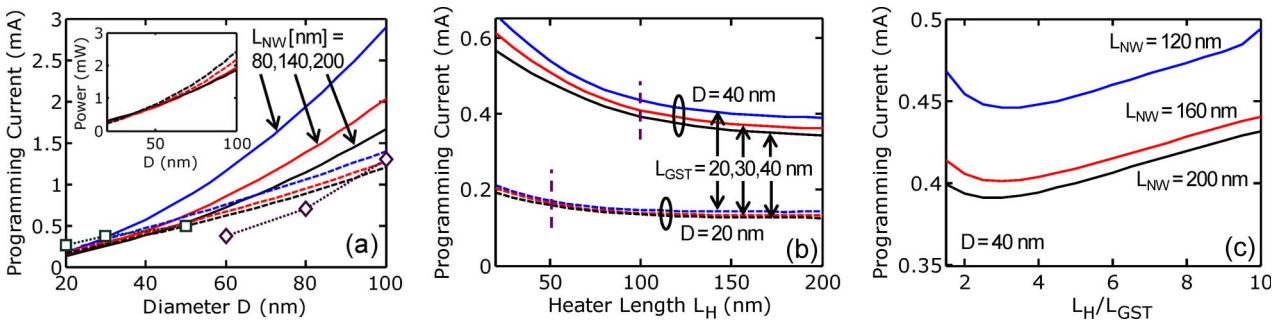

Fig. 3. Programming current dependence on geometric properties. (a) Varying diameter, with $L_{\rm NW}$ fixed for solid curves, where cell resistance is proportional to $1/D^2$. Aspect ratio $(AR = L_{\rm NW}/D)$ is fixed for dashed curves, where cell resistance is proportional to 1/D. Blue, red, and black dashed curves are for $AR = 3, 4, 5$, respectively. Related experimental data is taken from [12] (diamonds) and [19] (squares). (Inset) Diameter dependence of programming power. The analytical results agree with FE simulations within 10% for diameters down to 10 nm if fixed AR is assumed, and greater than 20 nm otherwise. (b) Varying heater length, for two diameters. L_H "knees" are indicated by vertical dashed lines (see text). (c) Varying heater–GST ratio reveals an optimum programming current.

However, we cannot assume a uniform lateral temperature within the GST, as its thermal conductivity is comparable to the surrounding SiO_2. We model the radial temperature as a quadratic, which is a good approximation to the heat diffusion equation [see (1)] with an internal heat source

$$T_G(r,z,t) = \begin{cases} T_G(0,z,t)+(T_G(R^-,z,t)-T_G(0,z,t))\left(\frac{r}{R}\right)^2, & r<R \\ T_G(R^+,z,t)\exp\left(-\frac{r^2-R^2}{4\alpha_{\rm SiO_2}t}\right)\frac{R}{r}, & r>R \end{cases} \tag{11}$$

with the boundary condition at $r = R$

$$\frac{T_G(R^-,z,t)-T_G(R^+,z,t)}{R_B^{\rm SiO_2-GST/TiN}} = -k_{\rm GST/TiN}\left.\frac{\partial T_G}{\partial r}\right|_{r=R^-} = -k_{\rm SiO_2}\left.\frac{\partial T_G}{\partial r}\right|_{r=R^+}. \tag{12}$$

By using the results from (8)–(10) and substituting (11) into (12), we can express $T_G(r,z,t)$ in terms of $T_G^{\rm hot}(t)$. $T_G^{\rm hot}(t)$ is then explicitly solved by taking advantage of the energy conservation law

$$I^2\frac{\rho_{\rm GST}L_G}{A}t = E_G(t) + \frac{E_H(t)+E_T(t)}{b} + cE_{\rm ox}^{\rm diff}(t) + E_{\rm TCu}^{\rm diff}(t) + E_{\rm BCu}^{\rm diff}(t) \tag{13}$$

where b accounts for the initial heating in TiN as in (6) and $c = 5L_G/(L_T + L_H - 0.25L_G)$ is an empirical parameter which accounts for spreading lateral heat loss from the NW to the Cu interconnect through the oxide.

The total temperature solution is finally obtained by superposing the heating from the bottom electrode $T_H(r,z,t)$, top electrode $T_T(r,z,t)$, and GST $T_G(r,z,t)$, such that the overall temperature distribution is $\Delta T(r,z,t) = T_H(r,z,t) + T_T(r,z,t) + T_G(r,z,t)$. The results of this model with default parameters [Fig. 1(b)] are shown in Fig. 2 and compared with comprehensive FE simulations. We note that the analytic model provides the correct temperature dependence in both temporal and spatial variations. The agreement with FE simulations is better than 10% at the key temperature points down to 10-nm NW diameters and correctly reproduces the temperature drops at boundaries due to TBR. In addition, the simulation time is reduced by approximately two orders of magnitude, enabling a novel and robust approach toward circuit simulation of the entire PCM memory arrays.

III. Sensitivity Analysis and Discussion

Based on the efficient thermal model described earlier, the minimum RESET current for the GST layer to reach melting temperature ($\Delta T \sim 600$ K) can be obtained by providing cell geometry parameters, material properties, and TBRs as in Fig. 1. The results are collected and shown in Fig. 3 for typical ranges of cell geometry and material properties. Once again, we have compared these results against FE simulations, finding agreement within 10%.

Fig. 3(a) shows the expected correlation between NW diameter and programming current. Solid lines show the case when the total cell length $(L_{\rm NW} = L_T + L_G + L_H)$ is fixed, while dashed lines show the case when the AR of cell segments is fixed, but the total NW length is varied. Stronger dependence is observed when $L_{\rm NW}$ is fixed. For the total programming power shown in the inset, this stronger dependence is cancelled by the inverse relationship with the electrical cell resistance, and all curves fall roughly on the same trend. Although our default material parameter set is somewhat generic, and not fit to any particular test structure, the confined GST cells of [12] and [19] demonstrate a very similar trend to our model when $L_{\rm NW}$ is fixed [symbols in Fig. 3(a)]. Additional data for GST NWs found in [14] also reveal a similar scaling trend, although a direct comparison with our model is more difficult due to the *horizontal* geometry and the much lower air/vacuum surrounding thermal conductance in such experiments. Our model is specifically focused on the *vertical* NW structure, which represents the more technologically relevant scenario (higher bit density). In practice, as with any physically based compact model, the exact material parameters must be treated as adjustable inputs and fit to the empirical data to account for specific materials and process conditions.

Extending the bottom heater length L_H can reduce the programming current as more energy is transferred to (and kept in) the GST layer. However, this is only effective up to a point,

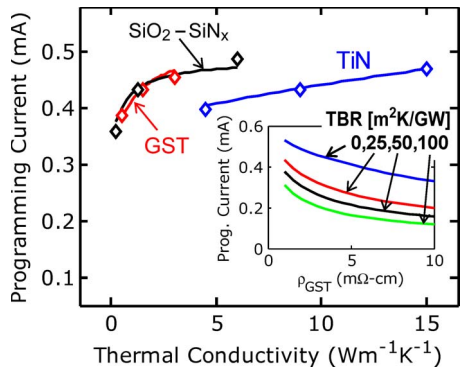

Fig. 4. Dependence of programming current on material properties, spanning typical ranges. Geometric parameters are $R = 20$ nm, $L_T = L_G = 20$ nm, and $L_H = 100$ nm. Solid lines represent compact model results, symbols are obtained from FE simulations (good agreement is found throughout). The inset shows dependence of programming current on TBR and GST resistivity, revealing the strongest dependence on the former.

as shown in Fig. 3(b). Extending L_H beyond the "knee" indicated by vertical dashes simply causes additional energy to diffuse out of the NW without efficiently heating the GST layer. Fig. 3(c) shows the interesting result of varying only the heater–GST ratio, with the top electrode length fixed at $L_T = 10$ nm. A minimum programming current is observed when the ratio $L_H/L_G \approx 2-4$. High ratio enables the "knee" effect as described above, while low ratio decreases the cell resistance due to the fact that $\rho_{\rm GST} < \rho_{\rm TiN}$. Thus, an optimum heater-GST aspect ratio is expected for a given top electrode thickness, cell diameter, and material property set.

Before concluding, we explore the model sensitivity to material and interface thermal properties in Fig. 4. These may be varied, in practice, by altering GST stoichiometry [16], replacing SiO_2 with other insulators (such as SiN_x), or changing the heater material (here, TiN). As shown, lowering thermal conductivity of all materials typically leads to better thermal confinement and reduced programming current. Excellent agreement is found between our compact model results (lines) and FE simulations (diamonds). Variations in temperature may also affect thermal properties, although this is more pronounced in *crystalline* materials below their Debye temperature (e.g., silicon, SiC, AlN, or carbon nanotubes) [17]. This is not the typical case for PCM, with amorphous or polycrystalline materials operating in the range of 300 K–900 K, typically above their Debye temperatures. Finally, we examine the role of TBR and GST resistivity in the Fig. 4 inset. The TBR for most materials is expected to fall approximately in the range of $0-100$ m^{2}K/GW [8]. Higher TBR is desirable in PCM, giving better thermal confinement and lower programming current. We note that the model predicts by far the most significant impact from increased TBR (up to $3\times$ lower RESET current) and smaller NW diameter [Fig. 3(a)] versus changes in other material parameters within their reasonably expected ranges. However, a reduced programming current is also obtained when the GST resistivity is increased, where we have correlated the electron contribution to GST thermal conductivity through the Wiedemann–Franz relation [17] as $k_{\rm GST} = k_0 + L_0 T/\rho_{\rm GST}$, where k_0 is the lattice contribution, T is the absolute temperature, and $L_0 = 2.44 \times 10^{-8}$ W $\cdot\, \Omega \cdot$ K^{-2} is the Lorenz number [18].

IV. Conclusion

In summary, we have developed an efficient compact thermal model to analyze the temperature distribution in segmented NW PCM cells, in both transient and steady-state time scales. The model is derived by solving the heat diffusion equation, including effects of TBR, and taking advantage of the cylindrical cell symmetry. The results agree with FE simulations within 10% error, at up to two orders of magnitude reduced computational time. The analytic solution offers physical insights into energy diffusion across materials and boundaries and allows us to quickly optimize the programming current with respect to cell geometry, material properties, and TBR. The model proposed here will also enable the efficient treatment of PCM cell arrays within circuit simulators such as SPICE.

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References

[1] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y.-C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S.-H. Chen, H.-L. Lung, and C. H. Lam, "Phase-change random access memory: A scalable technology," *IBM J. Res. Develop.*, vol. 52, no. 4/5, pp. 465–479, Jul. 2008.

[2] A. L. Lacaita, "Phase change memories: State-of-art, challenges and perspectives," *Solid State Electron.*, vol. 50, no. 1, pp. 24–31, Jan. 2006.

[3] A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, "Scaling analysis of phase-change memory technology," in *Proc. IEDM Tech. Dig.*, 2003, pp. 29.6.1–29.6.4.

[4] N. Yamada, E. Ohno, K. Nishiuchi, N. Akahira, and M. Takao, "Rapid-phase transitions of GeTe $-$ Sb_2Te_3 pseudobinary amorphous thin films for an optical disk memory," *J. Appl. Phys.*, vol. 69, no. 5, pp. 2849–2856, Mar. 1991.

[5] M. Wuttig and N. Yamada, "Phase-change materials for rewriteable data storage," *Nat. Mater.*, vol. 6, no. 11, pp. 824–832, Nov. 2007.

[6] A. Redaelli, A. Pirovano, F. Pellizzer, A.L. Lacaita, D. Ielmini, and R. Bez, "Electronic switching effect and phase-change transition in chalcogenide materials," *IEEE Electron Device Lett.*, vol. 25, no. 10, pp. 684–686, Oct. 2004.

[7] A. L. Lacaita, A. Redaelli, D. Ielmini, F. Pellizzer, A. Pirovano, A. Benvenuti, and R. Bez, "Electrothermal and phase-change dynamics in chalcogenide-based memories," in *Proc. IEDM Tech. Dig.*, 2004, pp. 911–914.

[8] J. P. Reifenberg, D. L. Kencke, and K. E. Goodson, "The impact of thermal boundary resistance in phase-change memory devices," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1112–1114, Oct. 2008.

[9] U. Russo, D. Ielmini, A. Redaelli, and A. L. Lacaita, "Modeling of programming and read performance in phase-change memories—Part I: Cell optimization and scaling," *IEEE Trans. Electron Device*, vol. 55, no. 2, pp. 506–514, Feb. 2008.

[10] J. P. Reifenberg, H. Gupta, M. Asheghi, and K. E. Goodson, "Closed form thermal analysis of phase change memory devices," in *ECI Int. Conf. Heat Transf. Fluid Flow Microscales*, Whistler, BC, Canada, 2008.

[11] B. Rajendran, J. Karidis, M.-H. Lee, M. Breitwisch, G. W. Burr, Y.-H. Shih, R. Cheek, A. Schrott, H.-L. Lung, and C. Lam, "Analytical model for RESET operation of phase change memory," in *Proc. IEDM Tech. Dig.*, 2008, pp. 1–4.

[12] D.-S. Chao, Y.-C. Chen, F. Chen, M.-J. Chen, P.H. Yen, C.-M. Lee, W.-S. Chen, C. Lien, M.-J. Kao, and M.-J. Tsai, "Enhanced thermal efficiency in phase-change memory cell by double GST thermally confined structure," *IEEE Electron Device Lett.*, vol. 28, no. 10, pp. 871–873, Oct. 2007.

[13] S. L. Cho, J. H. Yi, Y. H. Ha, B. J. Kuh, C. M. Lee, J. H. Park, S. D. Nam, H. Horii, B. K. Cho, K. C. Ryoo, S. O. Park, H. S. Kim, U.-I. Chung, J. T. Moon, and B. I. Ryu, "Highly scalable on-axis confined cell structure for high density PRAM beyond 256 MB," in *VLSI Symp. Tech. Dig.*, 2005, pp. 96–97.

[14] S. H. Lee, Y. Jung, and R. Agarwal, "Highly scalable non-volatile and ultra-low-power phase-change nanowire memory," *Nat. Nanotechnol.*, vol. 2, no. 10, pp. 626–630, Oct. 2007.

[15] S. Meister, H. Peng, K. McIlwrath, K. Jarausch, X. F. Zhang, and Y. Cui, "Synthesis and characterization of phase-change nanowires," *Nano Lett.*, vol. 6, no. 7, pp. 1514–1517, Jul. 2006.
[16] J. P. Reifenberg, M. A. Panzer, S. Kim, A. M. Gibby, Y. Zhang, S. Wong, H.-S. P. Wong, E. Pop, and K. E. Goodson, "Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films," *Appl. Phys. Lett.*, vol. 91, no. 11, p. 111 904, Sep. 2007.
[17] C. Kittel, *Introduction to Solid State Physics*, 8th ed. New York: Wiley, 2005.
[18] W. Risk, C. T. Reitner, and S. Raoux, "Thermal conductivities and phase transition temperatures of various phase-change materials measured by the 3ω method," *Appl. Phys. Lett.*, vol. 94, no. 10, p. 101 906, Mar. 2009.
[19] J. I. Lee, H. Park, S. L. Cho, Y. L. Park, B. J. Bae, J. H. Park, J. S. Park, H. G. An, J. S. Bae, D. H. Ahn, Y. T. Kim, H. Horii, S. A. Song, J. C. Shin, S. O. Park, H. S. Kim, U.-I. Chung, J. T. Moon, and B. I. Ryu, "Highly scalable phase change memory with CVD GeSbTe for sub 50 nm generation," in *Proc. VLSI Symp. Tech. Dig.*, Jun. 12–14, 2007, pp. 102–103.

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