VO_2 Switch for Electrostatic Discharge Protection

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***Abstract*—On-chip protection from electrostatic discharge (ESD) and electrical overstress (EOS) is a continuous challenge in the semiconductor industry, requiring significant design costs and die space. Insulator-metal transition (IMT) materials like vanadium dioxide (VO_2) could be used as bidirectional, compact voltage snapback devices for ESD protection that are not required to be in the front-end silicon. However, the reliability and response of these materials to ESD is not yet well studied. Here, we perform transmission line pulse (TLP) tests on thin film (50 – 150 nm) VO_2 devices. These can repeatedly sustain high currents in their metallic state, but still return to insulating once an ESD event is over. Devices with widths from 5 to 50 μm can carry a maximum current (I_{t2}) from ~1 to over 10 A, equivalent to ~1 to 15 kV of ESD protection. Furthermore, the snapback voltage can be engineered by varying the device length. These results suggest that IMT materials could be promising for use in on-chip ESD/EOS protection.**

***Index Terms*—Electrostatic discharge (ESD), insulator-metal transition (IMT), transmission line pulse (TLP), vanadium dioxide (VO_2), voltage snapback.**

I. Introduction

PROTECTING against electrostatic discharge (ESD) is an ongoing challenge in the manufacturing of electronics, with substantial cost implications [1]. ESD events occur when a build-up of charge is rapidly released into the pins of a chip due to contact with manufacturing/testing tools or human operators. Such events are characterized by large currents of several Amperes on time scales of nanoseconds, which can be extremely destructive to electronics. For example, ESD events can damage ultra-thin transistor gate dielectrics [2] or cause sudden failure of interconnects [3], [4], and are increasingly challenging when reducing these components to smaller dimensions [5]. The more general class of events, where the chip sees a higher voltage or current than it was designed to handle, is referred to as electrical overstress (EOS), and requires similar protection on larger time scales [6].

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To divert large ESD currents away from sensitive devices, on-chip ESD clamps must become conductive within nanoseconds, then return to insulating once the event has passed. Insulator-metal transition (IMT) materials like vanadium dioxide (VO_2) inherently have this behavior, with a drop in resistivity by several orders of magnitude once their transition temperature T_{IMT} is reached [7]. In two-terminal IMT devices, volatile resistive switching can be triggered at a critical voltage using Joule heating [8], which must be designed larger than the chip operating voltage when used for ESD protection. Using IMT-based voltage snapback devices for ESD protection is promising [9], especially because they are bidirectional, compact, and potentially back-end-of-line (BEOL) compatible, unlike traditional protection. Existing silicon-based solutions take up significant area [10] and moving to compact devices closer to the package pins could lead to significant cost and performance benefits. The required ratings for protection during ESD and leakage current during normal operation depend on a given chip's sensitivity and its environment, but $>$500 V protection under the human body model (HBM) is typical and $>$2 kV is ideal [11].

However, an understanding of IMT material behavior at the time scales and currents relevant to ESD is currently lacking. Here we use transmission line pulse (TLP) testing, an industry standard technique that emulates the short time scales and high energies of ESD events [12], to evaluate the snapback and current carrying capability (I_{t2}) of thin film VO_2 devices. Unlike DC measurements of VO_2 devices, which use a current compliance resistor and limit the accessible on/off ratio [13], TLP measurements do not have a current compliance and fully access the metallic "on" state of the device, in order to determine its failure point. These represent the highest current stress measurements (up to 10 A) of an IMT device to date. We also assess the sensitivity of TLP behavior to device geometry, finding that such IMT-based ESD devices are highly area-efficient compared to silicon-based diodes.

II. Devices

A schematic of the two-terminal VO_2 devices used for TLP testing is shown in Fig. 1(a), and a scanning electron micrograph (SEM) of a typical finished device is shown in Fig. 1(b). VO_2 thin films (with thickness t = 50, 100, 150 nm) were grown on c-plane sapphire substrates using physical vapour deposition (PVD) of a V_2O_5 target with Ar sputtering [14]. The VO_2 was patterned into rectangular stripes using optical lithography and CF_4/Ar dry etching (60 sccm CF_4, 30 sccm Ar, 5 mTorr, 500 W ICP power, 100 W bias power, ~50 nm/min etch rate). Contacts were defined by a second optical lithography step and electron-beam evaporation of 100 nm of Pd then 400 nm of Al, followed by

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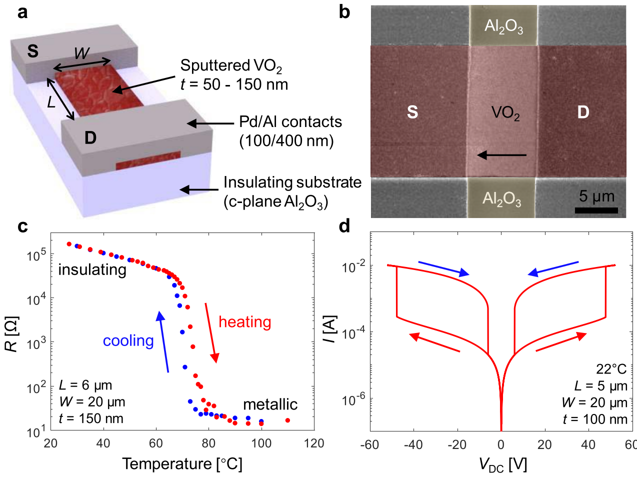

Fig. 1. (a) Diagram of a two-terminal VO_2 device used for transmission line pulse (TLP) testing. (b) Top view SEM image of a finished device ($W = 15$ μm, $L = 8$ μm, $t = 100$ nm). Arrow shows direction of current flow. (c) Measured resistance of a device as a function of temperature, with the VO_2 showing an insulator-metal transition (IMT) near $T_{IMT} \approx 70°C$. (d) Typical voltage-controlled DC characteristics of another VO_2 device, showing volatile, bidirectional switching.

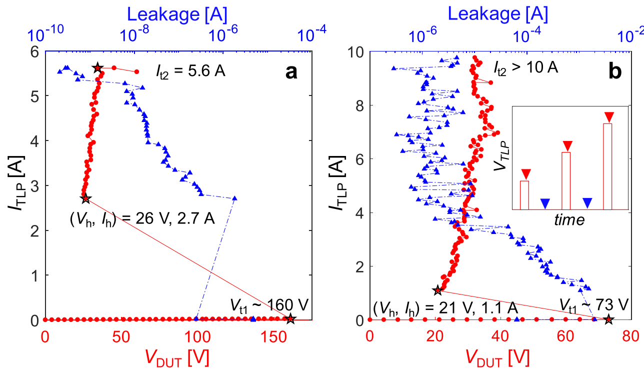

Fig. 2. (a) Representative TLP curve (red circles) for a VO_2 device ($L = 10$ μm, $W = 10$ μm, $t = 100$ nm), showing voltage snapback at V_{t1} due to IMT. The device eventually fails as open at a maximum current of $I_{t2} = 5.6$ A. Stars label the trigger voltage V_{t1}, hold voltage V_h, and failure I_{t2}. DC leakage (blue triangles) is measured at 5 V after each pulse, and decreases with increasing pulses. (b) TLP curve of a VO_2 device ($L = 6$ μm, $W = 50$ μm, $t = 150$ nm) that survived up to ~10 A of current (the instrument limit). The inset schematic shows when I_{TLP} and V_{DUT} (red) as well as leakage at 5 V DC (blue) are measured.

lift-off. SPR 220-3 photoresist with 3 μm thickness was used because of the poor selectivity of the dry etch, and to aid with lift-off. Devices tested had VO_2 widths of $W = 5$ to 50 μm and lengths of $L = 1$ to 15 μm, as shown in Fig. 1(a).

The temperature-dependent resistance of a VO_2 device is shown in Fig. 1(c), with the VO_2 displaying IMT near 70°C and a change in resistance by $>10^3\times$. Once it cools, the VO_2 returns to insulating, with a temperature hysteresis of ~5°C. Voltage-controlled DC switching is shown in Fig. 1(d). As the voltage increases (red arrow), the VO_2 is Joule-heated to its IMT temperature and it abruptly switches to the metallic state at $|V_{IMT}|$. After this point, the power dissipated in the device is much higher due to the lower resistance in the metallic state. Thus, the voltage must decrease much further (blue arrow) for the device to cool and return to its insulating state. In DC measurements a 5 kΩ resistor is used in series with the device as a current compliance to avoid damage due to overheating in the metallic state, limiting the on/off resistance ratio. Switching is repeatable and bidirectional, i.e. independent of voltage polarity in all devices measured.

III. Transmission Line Pulse (TLP) Testing

Fig. 2 displays TLP testing done at room temperature by inputting a series of 100 ns square pulses with 10 ns rise and fall times into the device under test (DUT) with increasing voltage, until the device failed. Voltage (V_{DUT}) and current (I_{TLP}) in the DUT were measured between 70 to 90 ns on the output TLP waveform. The pulse rate was ~10/min (the device had time to cool between pulses), and DC leakage current was measured at 5 V between pulses, to assess degradation. No current compliance was used.

TLP curves (red) with post-pulse DC leakage (blue) for typical VO_2 devices are shown in Fig. 2, with the inset schematic showing when each measurement is taken. The leakage is plotted along the top axis, as a function of I_{TLP} (vertical axis). The VO_2 remains in its insulating state until it undergoes an IMT to the metallic state at V_{t1}, triggering a voltage snapback to $V_h \sim 25$ V (the snapback is due to the device's change in resistance and therefore its impedance mismatch with the transmission line or ESD source). This is accompanied by an increase in current by several orders of magnitude. Once each pulse is over, the VO_2 returns to its insulating state due to the volatile nature of its IMT, confirmed by the post-pulse leakage. Stressing the device similar to an ESD event, each pulse with $V > V_{t1}$ triggers an IMT. Beyond I_{t2} the device fails as open and is no longer capable of an IMT and voltage snapback. All measured devices show similar TLP characteristics regardless of bias polarity, handling both positive and negative ESD events.

The VO_2 devices can carry a maximum current I_{t2} ranging from ~1 to over 10 A (the instrument limit), surviving from ~2 ESD-like TLP switching events in smaller devices to >100 in the larger devices tested. (Even surviving a handful of ESD events is sufficient for device qualification.) This is equivalent to ESD protection of ~1 to 15 kV under the human body model [15]. Assuming a uniform current flow, this suggests current densities of ~100 to 950 MA/cm^2 in the VO_2 strip. However, the IMT is likely initiated in a localized "filament" where the VO_2 is hottest [16], meaning the actual current densities and local temperature rises are much higher. For comparison, typical Cu, Al, or CuAl interconnects can carry ~70 to 150 MA/cm^2 when tested under the HBM [4], [17]–[19].

The insulating state leakage of the VO_2 typically starts near several μA, and is smaller in narrow devices. After the first TLP to trigger snapback, leakage can either increase or decrease slightly. As the device is subjected to more TLP, leakage decreases (Fig. 2) due to increasing damage to both the VO_2 and the contacts, until failure as an open.

If TLP testing is stopped well before failure, or the ~10 A limit is reached without failure [e.g. in Fig. 2(b)], then the VO_2 still shows temperature-induced IMT and DC switching behavior, but with lower performance. Fig. 3(a) shows voltage-controlled DC switching behavior with a 5 kΩ series resistor for the device in Fig. 2(b) before and after TLP. There is still bidirectional, volatile switching, but the switching voltage has increased (likely due to changes in current flow and self-heating). Fig. 3(b) shows that IMT is still present near 70°C, but it is less sharp and lower in magnitude, indicat-

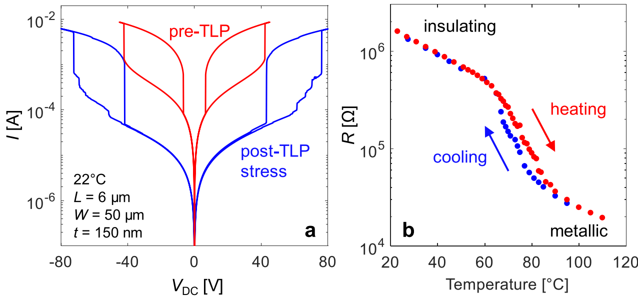

Fig. 3. (a) DC voltage-controlled switching of the device in Fig. 2(b) before (red) and after (blue) TLP. Despite having carried ~10 A, the device still shows volatile bidirectional switching after TLP. (b) Resistance of the same device as a function of temperature after TLP measurements. There is still an IMT, but with reduced magnitude and abruptness.

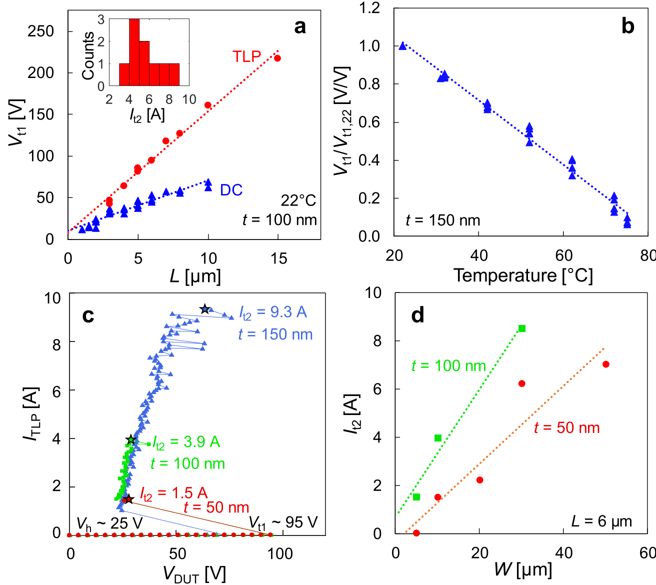

Fig. 4. (a) Room temperature switching voltage V_{t1} in DC (blue triangles) and TLP (red circles) increases linearly with device length. The inset shows the distribution of I_{t2} values measured in the TLP devices corresponding to the red circles ($W = 10\ \mu$m, $t = 100$ nm). (b) DC V_{t1} normalized to V_{t1} at 22°C reduces with increasing ambient temperature ($L = 1$ to $15\ \mu$m). (c) TLP curves for devices with different thicknesses ($L = 6\ \mu$m, $W = 10\ \mu$m). V_{t1} and V_h are unaffected, but I_{t2} improves with increased thickness. (d) I_{t2} from TLP for VO_2 devices with different widths and thicknesses. Dashed lines represent linear fits.

ing changes to at least part of the VO_2 channel. Further study is needed to better understand the origin of these changes.

Fig. 4(a) shows that device switching voltage V_{t1} in both DC and TLP decreases linearly with reducing device length. This occurs because shorter devices have lower resistance, requiring lower voltages to reach the IMT temperature. Linear fits give a slope of 14.6 ± 0.6 V/μm and 6.1 ± 0.3 V/μm for TLP and DC switching, respectively. For all devices, the switching voltage in TLP is roughly double the DC switching voltage. Since the time scales of TLP are much shorter than DC, device heating at a given voltage is much lower. Thus, higher voltages are needed to reach the IMT temperature during TLP. The vertical axis intercept ~8 V is primarily associated with contact resistance (~200 k$\Omega \cdot \mu$m when insulating) and heat loss at the contacts, and may represent a minimum DC switching voltage [20]. Reducing contact resistance to the VO_2 is expected to reduce this intercept [21], enabling sub-8 V applications.

Length appears to have no impact on I_{t2} or reliability for the range of devices measured. Thus, length provides a simple way of engineering the ESD clamp's trigger voltage to be above the chip operating voltage. The distribution of I_{t2} values measured for the TLP devices in Fig. 4a is shown as an inset, with a mean of 5.7 A and standard deviation of 1.4 A.

The DC switching voltage V_{t1} decreases by 1.7% per 1°C increase in ambient temperature, extracted from a linear fit to Fig. 4(b). This shift is reported as a percentage because its absolute magnitude depends on device length. The V_{t1} shift is partly due to the reduced temperature rise and therefore power required to reach the IMT. The large temperature coefficient of resistance (TCR) of the VO_2 in its insulating state also contributes to a reduction in V_{t1}, because of increased self-heating, and to an increase in leakage current with increasing temperature. For ESD protection devices, this means that the DC V_{t1} must be designed higher than the chip operating voltage with a margin to account for any increases in chip temperature.

Fig. 4(c) shows I_{t2} improves with increasing VO_2 thickness, with minimal impact on V_{t1}. Similarly, Fig. 4(d) shows that using wider devices results in higher I_{t2} and survival of more ESD events, but this comes at the cost of higher leakage current. Linear fits give approximate slopes of 220 ± 60 V/μm and 400 ± 60 V/μm under the HBM model [15] for the 50 nm and 100 nm films, respectively. This is highly area-efficient compared to ~20 to 80 V/μm for silicon-based diodes [10], [22], [23], and is expected to improve with increasing thickness or potential BEOL integration.

Further study of the failure mechanism in VO_2 devices is needed, which might be due to defect migration (e.g. oxygen vacancy migration [24], changes to the VO_2 stoichiometry [25], or voids) or in part to contact degradation. It is expected that I_{t2} could be improved by reducing the local temperature in the device. This could be done by adding electrically insulating but thermally conductive heat spreading layers next to the VO_2, e.g. Al_2O_3, AlN, or h-BN [26]. However, because the IMT is thermally driven, this would increase V_{t1}. Finally, we note that although our existing devices survive sufficiently many ESD events to be of practical use, their robustness could be further improved by increasing device dimensions (thickness and width) and improving their contacts.

IV. Conclusion

Materials with an IMT could enable the development of highly compact devices for bidirectional ESD protection, with the potential to be implemented in the back-end for silicon area savings. Here, we have assessed the current carrying capability of VO_2 as a prototypical IMT material for ESD protection, using TLP measurements. VO_2 devices can sustain several Amperes of current and repeatably undergo IMT in response to ESD-like energies. For ESD protection of chips with higher operating temperatures than 70°C or lower leakage requirements, other IMT materials with a higher band gap and transition temperature, and lower TCR in the insulating state, could be explored, such as NbO_2 [27], [28].

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